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A PHASE LOCKED
TONE BURST
GENERATOR

by

© GERALD W. GRANT

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH
IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE
OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING, 1973

THE UNIVERSITY OF ALBERTA
FACULTY OF GRADUATE STUDIES AND RESEARCH

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled "A Phase Locked Tone Burst Generator", submitted by Gerald W. Grant in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

A device has been constructed which generates tone bursts with trapezoidal envelope shapes. The tone burst is produced by amplitude modulating a sinusoidal carrier with a trapezoidal envelope signal. The frequency of the sinusoidal carrier and the trapezoid rise, fall, and plateau duration times are variable. A digitally programmable phase locked loop is used to generate the sinusoid. Provision is made to enable the sinusoid frequency to be computer-controllable. The trapezoid is generated by an analog circuit which is digitally controlled. A trigger circuit is included to ensure that the tone burst is always initiated at a point of zero phase relative to the sinusoid generated by the phase locked loop.

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LIST OF SYMBOLS

t - time

$x(t)$ - arbitrary envelope signal, generalized variable

ω_o - angular frequency of the sinusoid carrier, angular frequency of the phase locked loop output

ϕ - phase of the sinusoid carrier

$b(t)$ - composite input signal or tone burst

ω_r - angular frequency of the reference frequency

θ_r - phase of the reference signal

$e(t)$ - phase comparator output error signal

θ_o - phase of the phase locked loop output sinusoid

ω^* - angular frequency of the feedback signal

θ^* - phase of the feedback signal

N - value of the integer programmed into the $\div N$ counter

ω_v - angular frequency of the voltage controlled oscillator

ω_L - angular frequency of the local oscillator

$y(t)$ - mixer output

k_p - phase comparator gain constant

k_v - voltage controlled oscillator sensitivity to the filtered error signal

k'_v - voltage controlled oscillator sensitivity to the coarse tuning voltage

k_f - loop filter gain constant

$F(s)$ - loop filter gain constant

s - Laplace transform variable

a - zero position of the loop filter transfer function

ω_n - phase locked loop undamped natural frequency

ζ - phase locked loop damping ratio

K^* - lumped phase locked loop gain

$\Delta\theta$ - magnitude of theoretical phase step

$\Delta\omega$ - magnitude of theoretical frequency step

$M(s)$ - phase locked loop transfer function

I_s - magnitude of current source current

C - capacitance of trapezoid generator holding capacitor, capacitance of the loop filter capacitive element

$V_{cap}(t)$ - voltage on the trapezoid generator holding capacitor

$V_i(s)$ - Laplace transform of the loop filter input voltage

$V_o(s)$ - Laplace transform of the loop filter output voltage

$V_s(s)$ - Laplace transform of the loop filter summing junction voltage

$I_i(s)$ - Laplace transform of the loop filter input current

$I_f(s)$ - Laplace transform of the loop filter feedback current

R_2 - resistance of the loop filter feedback resistor

R_1 - resistance of the loop filter input resistor

$\delta(\omega)$ - Dirac delta function

CHAPTER 1

INTRODUCTION

Much research is being done to learn how the auditory system functions. Although the anatomical structure of the auditory system is well known, there is as yet no satisfactory model of the auditory system that lends itself to mathematical analyses. In other words, no satisfactory transfer function has been found.

One experimental method used in auditory research is the study of evoked neural responses. These are the responses of the auditory neurons that arise from known acoustic stimuli. The neural responses are obtained by implanting electrodes in or among the neurons. So far, such animals as guinea pigs, cats, and rats have mainly been studied. Few results are available for human subjects as surgery is required to implant the electrodes.

Various types of stimuli have been used. These include clicks, pulse trains, noise, and tone bursts. Most work has been done using tone bursts. A tone burst consists of a sinusoid which is amplitude modulated with various signals to produce a burst with an envelope of a guassian shape, a trapezoidal shape, etc.

Steady tones are not acceptable as inputs, as the physiological processes of fatigue and adaptation can influence the system response. A tone burst of sufficiently short duration (less than about 500 milliseconds) will not produce these effects; but a tone burst with a rectangular envelope is also not satisfactory since the rapid rise and fall of the envelope causes an

abrupt transient response to occur.[1,2] A trapezoidal envelope avoids the transient phenomenon.

There is, however, a problem with using simple envelope modulation of a sinusoid to produce a tone burst. If the sinusoid is given and the envelope signal is allowed to begin at a random time, a randomness will be introduced into the tone burst. To illustrate, suppose an arbitrary envelope signal, x(t), is to be used, and this is to be initiated at a random time (t=0) relative to the phase of the sinusoid. That is, if the sinusoid is given as $\sin(\omega_o t + \emptyset)$, where ω_o is the angular frequency, t is time measured from the beginning of x(t), and $\emptyset$ is phase angle, then $\emptyset$ will be a random variable. These functions are illustrated in Figure 1.1.

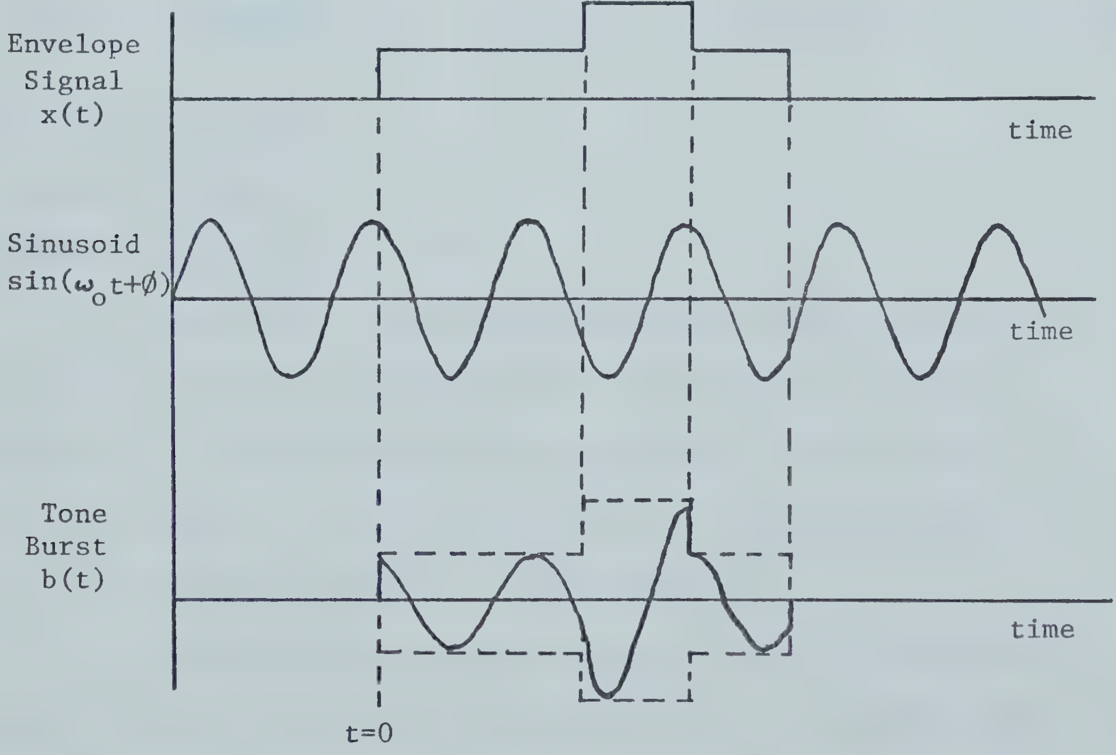


Figure 1.1 Illustration of Waveforms

A difficulty is thereby encountered. Goldstein[3] has shown that the ear is sensitive to phase for certain stimuli in monaural stimulation. Moreover, binaural stimulation is often used. It is not known if the phase sensitivity is significant when trapezoidal tone bursts are used.

The composite signal or tone burst, b(t), is given by:

$$b(t) = \left[x(t)\right] \cdot \left[\sin(\omega_0 t + \phi)\right]$$

In this case the Fourier transform of the composite signal will be given by:

$$\mathfrak{F}\left\{b(t)\right\} = \mathfrak{F}\left\{\left[x(t)\right] \cdot \left[\sin(\omega_0 t + \phi)\right]\right\} ,$$

where $\mathfrak{F}\{\}$ represents the Fourier transform.

This expression expands to (refer to Appendix A):

$$B(\omega) = (\cos\phi)(\pi/j)\left[X(\omega - \omega_0) - X(\omega + \omega_0)\right] + (\sin\phi)(\pi)\left[X(\omega + \omega_0) + X(\omega - \omega_0)\right]$$

where $B(\omega) = \mathfrak{F}\left\{b(t)\right\}$

and $X(\omega) = \mathfrak{F}\left\{x(t)\right\}$

and ω is the frequency variable.

Since ϕ is a random variable, it is evident that the transform is also of a random nature. If the burst is always initiated at the same phase of the sine wave, this randomness will be eliminated. For the design that is described in this thesis, this phase was chosen as zero degrees.

If the trapezoidal envelope can be made to begin and end at a point of zero phase of the sine wave, any possible phase effects will be eliminated. A device capable of producing this

type of signal is not available commercially.

The objective of the work reported in this thesis was to design, build, and evaluate such a device.

CHAPTER 2

THE BASIC SYSTEM

2.1 The Basic System Organization

The tone burst generator that was constructed was required to meet other specifications as well as to satisfy general requirements mentioned in Chapter 1.

The frequency of the sine wave was to be variable. External or internal burst triggering was to be available. The output burst amplitude was also to be variable.

These requirements suggested a phase locked system. This type of system was indeed constructed. The basic form of the system is shown in Figure 2.1.

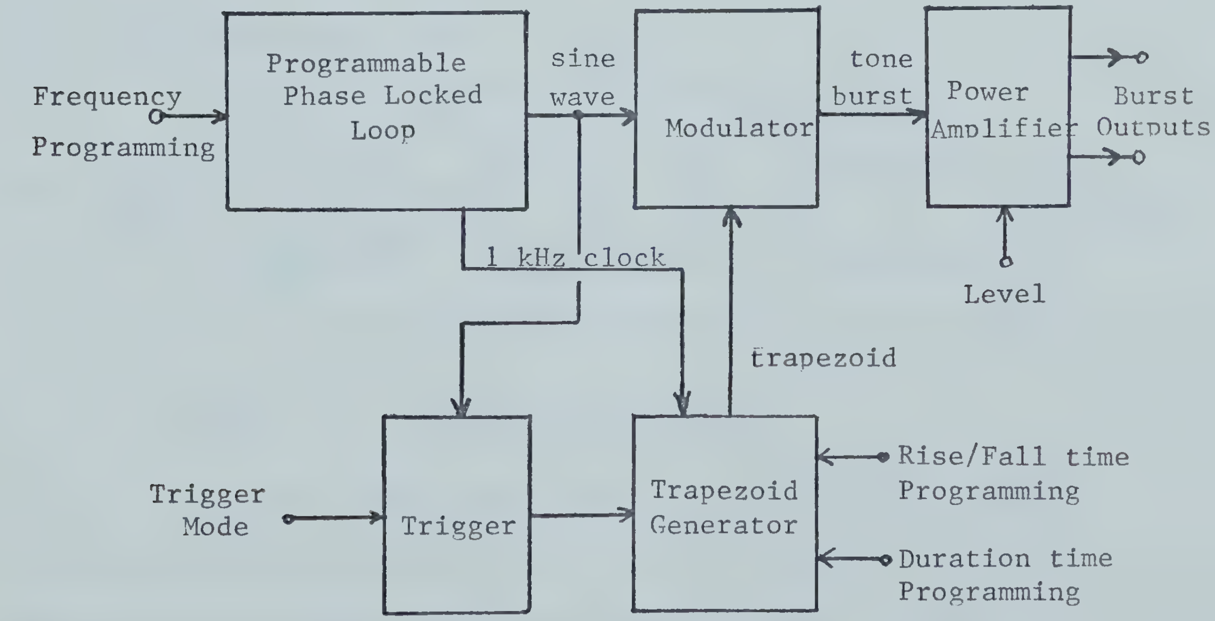


Figure 2.1 Basic Form of System

The digitally programmable phase locked loop generates a sinusoidal voltage which is fed to an amplitude modulator circuit. The trapezoid generator produces a trapezoidal voltage which is also fed to the modulator. Amplitude modulation is performed by the modulator circuit. The composite signal will be tone bursts. This signal is amplified by the power amplifiers. The power amplifier outputs are brought out for external use.

The 1kHz clock signal is generated by the phase locked loop and is fed to the trapezoid generator circuit. This signal is used to time the generation of the trapezoid. A trapezoid is generated when the trapezoid generator receives a "Triggered" pulse from the trigger circuit. The sinusoid is fed to the trigger circuit to ensure that the trapezoid begins at a point of zero phase.

2.2 The Phase Locked Loop

A basic phase locked loop is shown in Figure 2.2.

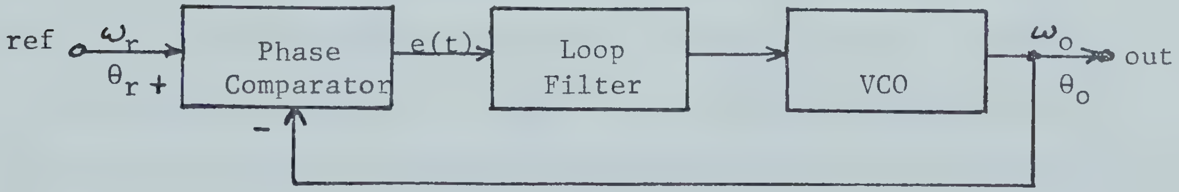


Figure 2.2 Basic Phase Locked Loop

The basic phase locked loop can be viewed as a simple feedback control system where phase is the variable of interest. The voltage controlled oscillator (VCO) generates an output of angular frequency ω_v and phase θ_v. This is fed back to a phase comparator. The phase comparator produces an output error signal,

e(t), which is proportional to the phase difference between the voltage controlled oscillator output and a reference signal of angular frequency ω_r and phase θ_r. The phase comparator output is filtered by the loop filter and tunes the voltage controlled oscillator. This system establishes ω_v equal to ω_r and θ_v locked to θ_r.

The voltage controlled oscillator can be made to produce a frequency other than ω_r by including a divide by N counter in the feedback path. This situation is illustrated in Figure 2.3.

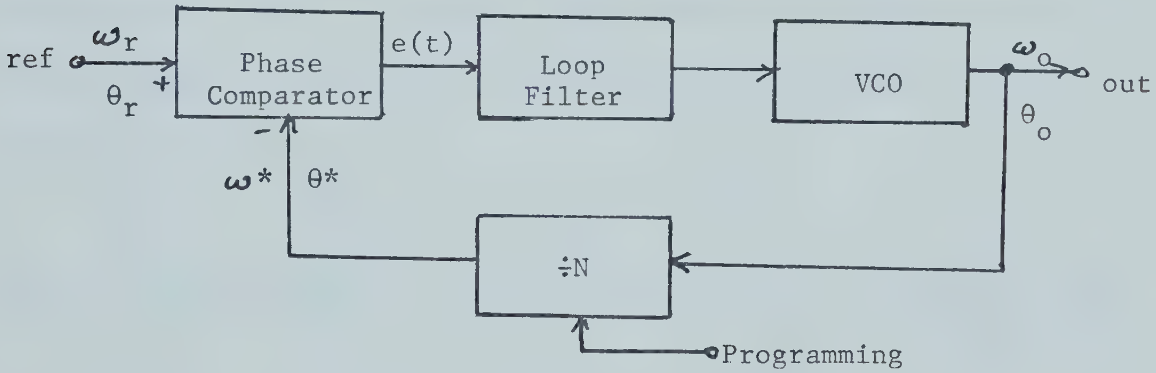


Figure 2.3 Phase Locked Loop with ÷N Counter

In this system, the output of the ÷N counter, of angular frequency ω^* and phase θ^*, is phase locked to the reference. The ÷N counter divides the output frequency (and phase, to first order[5]) by the factor N. Consequently, the output frequency of the voltage controlled oscillator must now be $N \cdot \omega_r$. By programming different values of N into the counter, various output frequencies can be generated.

For this application, a range of output frequencies of from 100 Hz to 20 kHz was required. With the system shown in Figure 2.3, the voltage controlled oscillator must operate over

this entire range. Practical oscillators operate poorly if at all over a range this large. If the output of the voltage controlled oscillator is mixed with the output of a local oscillator (LO), of angular frequency ω_L, and the difference frequency is extracted, this difficulty can be overcome. This scheme allows the voltage controlled oscillator and the local oscillator to operate at higher frequencies. The output signal, of angular frequency ω_o and phase θ_o, will now be different from the voltage controlled oscillator output. The voltage controlled oscillator now need vary only a relatively small amount to produce the required range of frequencies. This arrangement is illustrated in Figure 2.4.

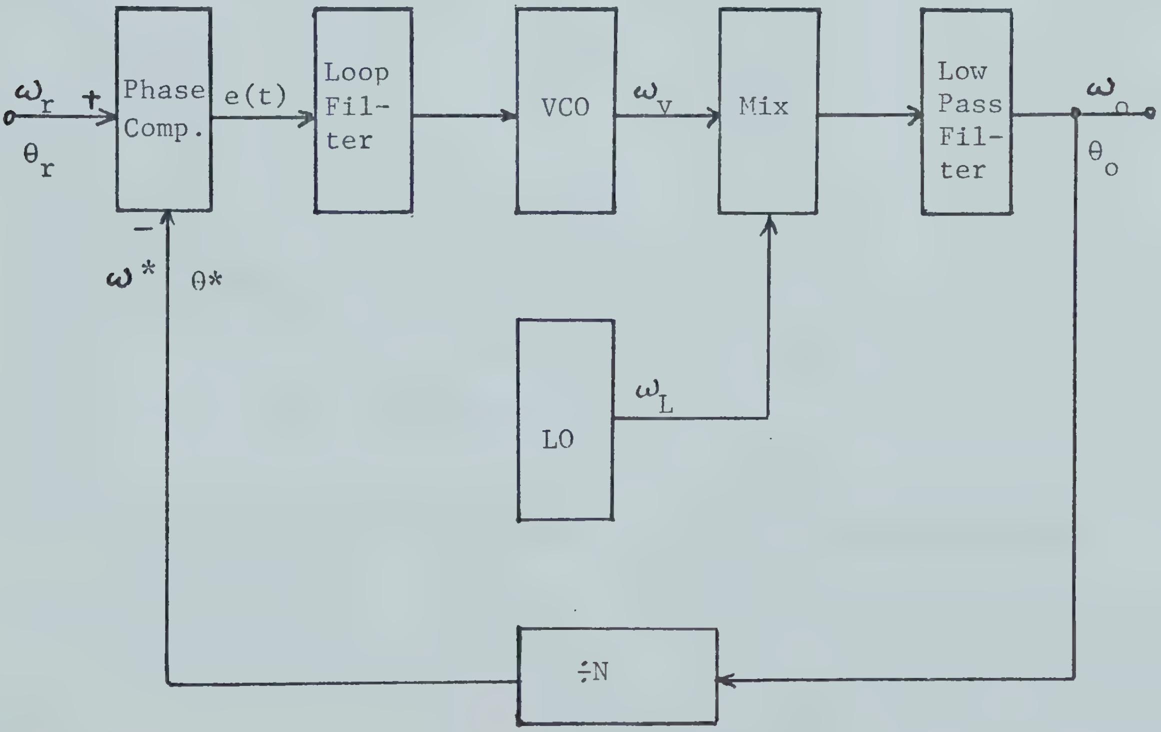


Figure 2.4 Phase Locked Loop with Mixer

The reference frequency must be obtained from some source. If the frequency of the local oscillator is chosen as 256 kHz, this signal can be divided down with digital counters to yield the reference signal. If the reference frequency is chosen as 100 Hz, the output frequency range will be covered in 100 Hz intervals. This was considered satisfactory. Consequently, The local oscillator frequency was divided by 16, by 16 again, and then by 10. The resulting system is shown in Figure 2.5.

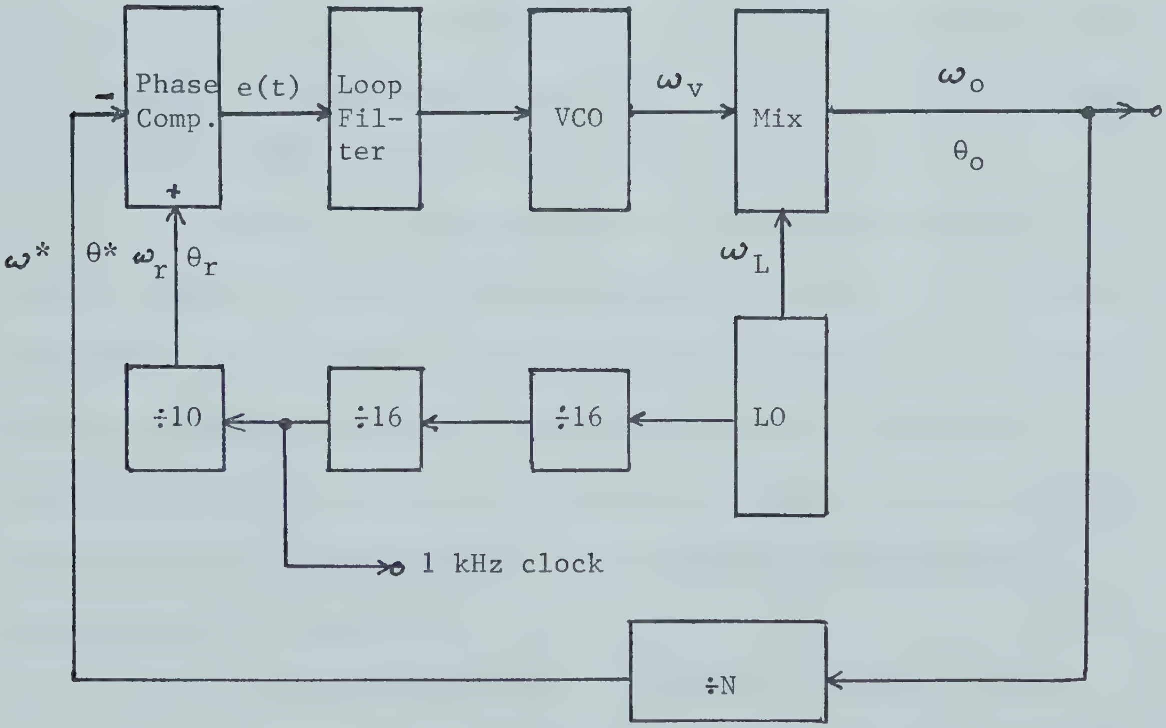


Figure 2.5 Generation of Reference Frequency

The two divisions by 16 result in a division by 256. Therefore, the output of the second ÷16 conter is a 1 kHz waveform. This signal is the "Clock" signal and is fed to the trapezoid generator circuit. The Clock signal and the loop output are both harmonically phase locked to the 100 Hz reference signal.

The particular design of the ÷N counter causes the counter to divide by 2N rather than by N. Consequently, the reference frequency must be divided by an additional factor of two to compensate for this. An additional ÷2 was placed after the ÷10 counter.

Some signal processing was required at various points. The output of the mixer and the local oscillator are sinusoids but are required to drive digital circuitry. Therefore, Schmitt trigger circuits were required before the digital circuitry.

A digital to analog converter is fed the programming of the ÷N counter. The output of this circuit is fed to the voltage controlled oscillator and coarse tunes the oscillator to a frequency near the frequency required. This scheme reduces the required tuning sensitivity of the voltage controlled oscillator and results in improved noise performance. The complete phase locked loop is illustrated in Figure 2.6.

The "squared" sine wave is fed to the trigger circuit. This signal is used to ensure that the trapezoid is always initiated at a point of zero phase.

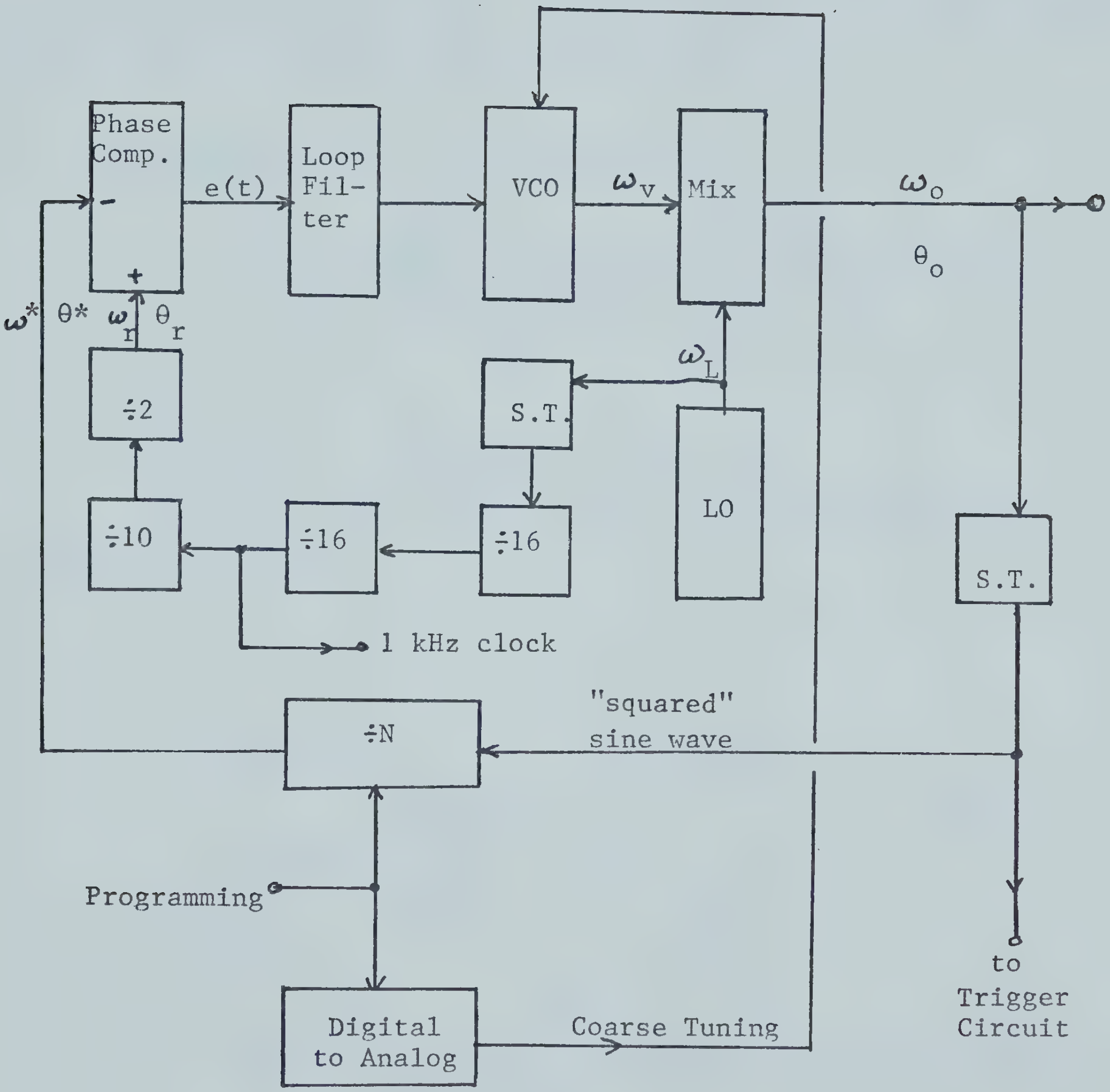


Figure 2.6 Complete Phase Locked Loop

2.3 The Trapezoid Generator

The generated trapezoid was to have controllable rise and fall times as well as a controllable plateau duration time. The rise and fall times were to be equal. The peak amplitude was to be constant as well. These times are illustrated in Figure 2.7.

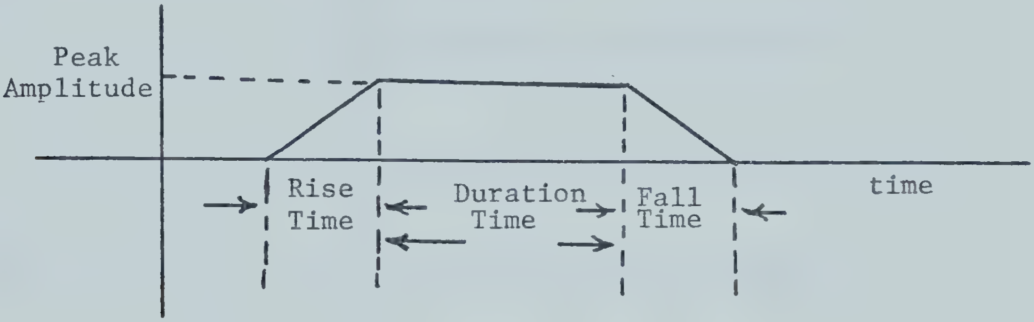


Figure 2.7 Illustration of Trapezoid

The basic organization of the trapezoid generator section is shown in Figure 2.8.

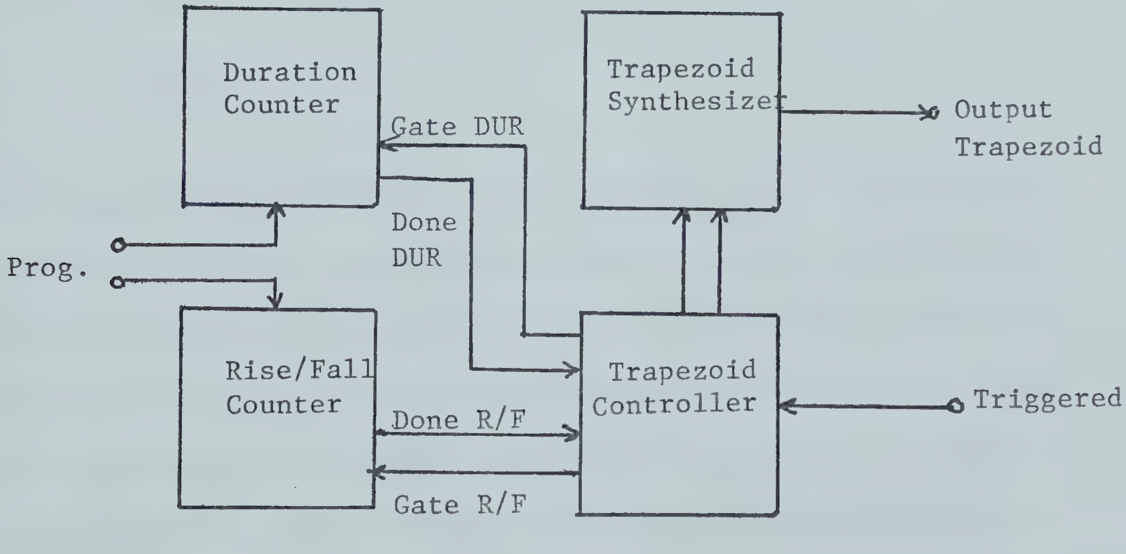


Figure 2.8 Trapezoid Generator Organization

The trapezoidal waveform is generated by the "Trapezoid Synthesizer". This circuit consists of two switched current sources of equal magnitude that charge and discharge a capacitor. This scheme is illustrated in Figure 2.9.

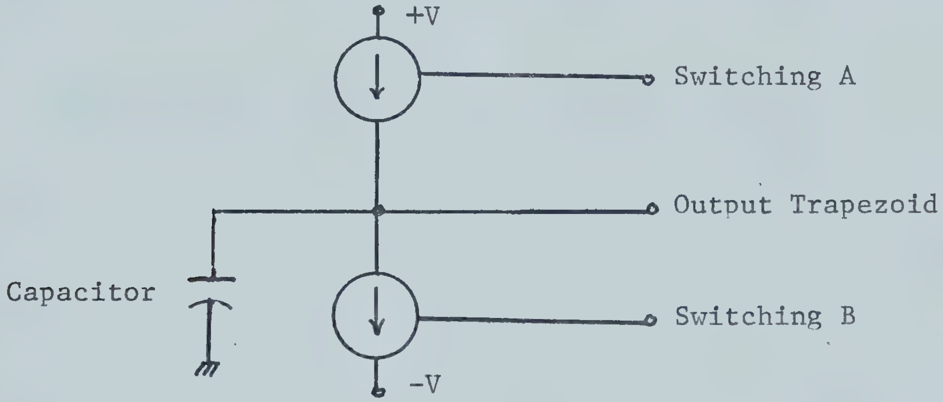


Figure 2.9 Trapezoid Generator Current Sources

The trapezoidal waveform is produced by switching the current sources on and off. The equation describing the charging (or discharging) of a capacitor by a current source is:

$$V_{cap}(t) = \frac{I_s\ t}{C_c} ,$$

where $V_{cap}(t)$ is the voltage on the capacitor, I_s is the value of the charging current, C_c is the capacitance of the capacitor, and t is time. When only one current source is operating, the voltage on the capacitor will be linearly increasing (or decreasing) with time. By properly switching the two current sources, a trapezoid can be generated. The switching sequence for a negatively going trapezoid is shown in Figure 2.10.

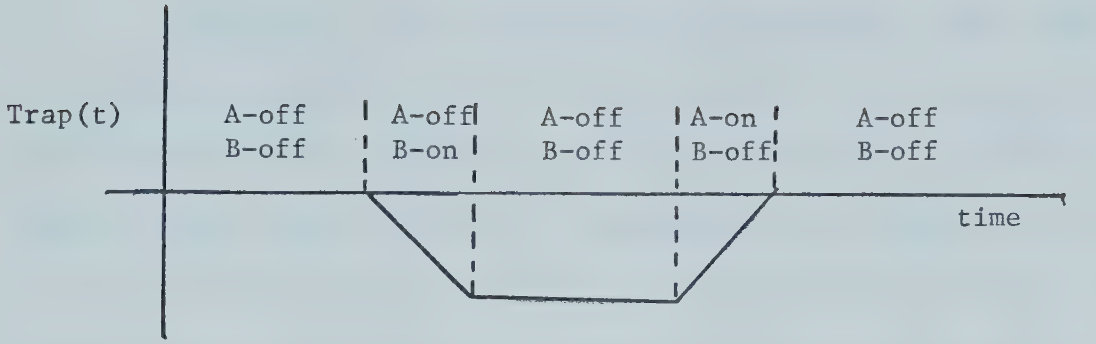


Figure 2.10 Current Source Switching Sequence

Proper timing is required to generate a trapezoid with specified rise/fall times and plateau duration time. The current sources are controlled by the "Trapezoid Controller" (refer to Figure 2.8). The switching times are determined by the two programmable counters shown in Figure 2.8. The required rise/fall and duration times are programmed into these counters. When the trapezoid controller receives a Triggered pulse from the trigger circuit, a switching sequence is initiated. The trapezoid controller gates the appropriate counter "ON", and this counter begins to count down from its programmed value. Since the 1 kHz clock signal drives the counters, 1 millisecond intervals are measured off. After the programmed time has elapsed, the counter sends a "DONE" pulse to the trapezoid controller. This circuit will then advance to the next required switching operation. The trapezoid controller continues to provide the required switching sequence, all the while being timed by the counters, until the complete trapezoid has been synthesized. When the entire sequence has been completed the trapezoid controller is ready for another Triggered pulse.

Since the 1 kHz clock signal is harmonically phase locked to the 100 Hz reference and the output sinusoid is also harmonically phase locked to the reference, then the trapezoid will be "phase locked" to the output sinusoid. Consequently, the trapezoid will end at a point of zero phase of the sinusoid if an integral multiple of the period of the sinusoid is equal to the total of the rise, fall, and duration times. That is, if an integral number of cycles of the sinusoid will exactly "fit" within the trapezoid, then the system will ensure that the trapezoid ends at a point of zero phase.

The output trapezoid must have a constant peak amplitude independent of the rise/fall times. The equation describing the charging of a capacitor by a current source was given as:

$$V_{cap}(t) = \frac{I_s \, t}{C_c}$$

This equation shows that if a constant charging current is used and a varying charging time is employed, then a varying peak value of $V_{cap}(t)$ will be obtained. This situation can be remedied by employing a gain control circuit. If a digital to analog converter is fed the programming of the rise/fall counter, then a voltage will be available which can be used to set the gain on the gain control circuit. This circuit either amplifies or attenuates (which ever is appropriate) the synthesized trapezoid such that the trapezoid output from the gain control circuit will have a constant peak amplitude, independent of rise/fall times. The complete trapezoid generator section is shown in Figure 2.11.

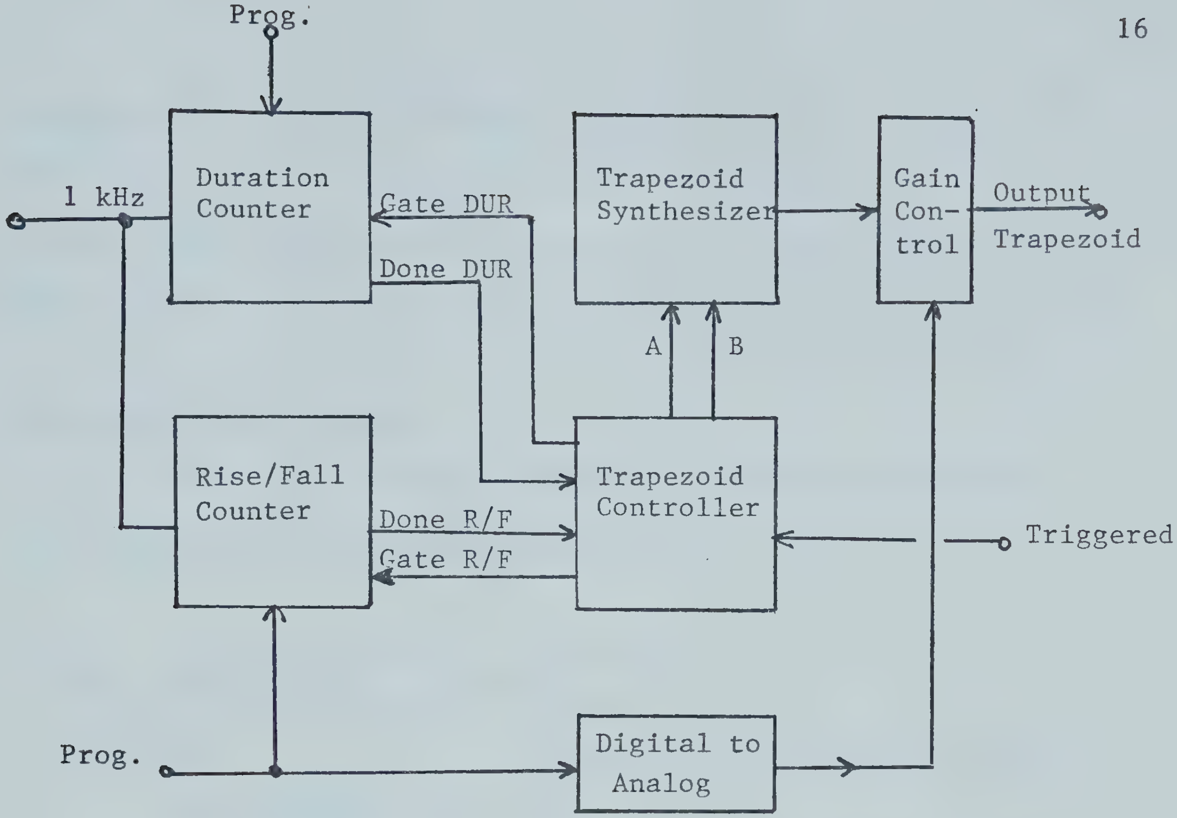


Figure 2.11   Complete Trapezoid Generator

2.4   The Modulator

The modulator is required to amplitude modulate the sine wave generated by the phase locked loop with the trapezoid generated by the trapezoid generator. Amplitude modulation is an analog multiplication process. Consequently, an integrated circuit analog multiplier was used.

2.5   The Power Amplifiers

Two output channels with separately variable output levels were required. Consequently, two power amplifiers were required. The input to each amplifier is the tone burst produced by the modulator.

The power amplifiers are of an operational amplifier

configuration. Switched feedback elements were used to vary the output power levels. Ten power levels are available, at 5 db spacing, with the lowest power level (0 db) being 50 μw into 8 ohms. The highest power level (45 db) is approximately 1½ watts into 8 ohms.

2.6 The Trigger Circuit

The trigger circuit triggers or initiates a tone burst. This system is illustrated in Figure 2.12.

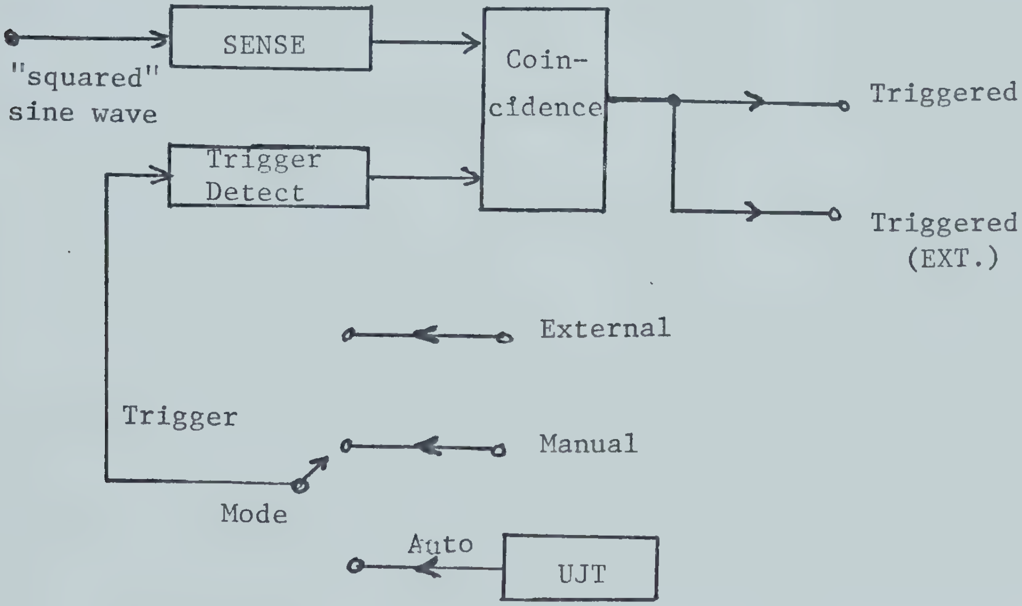


Figure 2.12 Trigger Circuit

Two conditions must be met before a burst is triggered. First, a "Trigger" pulse must occur. This pulse can originate from one of three sources, depending upon the trigger mode selected. This pulse can originate from an external source, a manual push-button, or a local low frequency unijunction transistor oscillator. This Trigger pulse is detected by the "Trigger Detect" circuit.

Second, the generated sine wave must be at a point of zero phase. This point is detected by the "Sense" circuit.

The outputs of the Sense circuit and the Trigger Detect circuit are fed to the "Coincidence" circuit. When both a trigger pulse and a zero phase condition have occurred, the Coincidence circuit produces an output "Triggered" pulse. This pulse is fed to the trapezoid controller and initiates a tone burst. The "Triggered" pulse is brought out for external use.

CHAPTER 3

PHASE LOCKED LOOP DESIGN

3.1 Introduction

The physical implementation of the phase locked loop was illustrated in Figure 2.6. Each block in Figure 2.6 can be represented by a mathematical model. When each block has been modelled, a loop transfer function can be obtained. The loop transfer function can be used to find the steady/state and transient response of the phase locked loop, and thereby tailor the system to meet specified performance criteria.

3.2 Derivations of Models

3.2.1 The Phase Comparator

The phase comparator produces an output voltage, e(t), proportional to the difference in phase of the two input waveforms. Consequently, this circuit can be represented as a summing junction with a gain, k_p. This is illustrated in Figure 3.1.

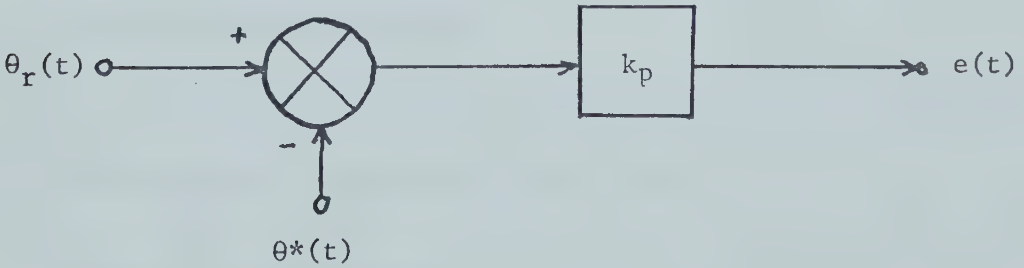


Figure 3.1 Phase Comparator Model

It is possible to write an equation describing the phase comparator operation. This will be:

$$E(s) = k_p(\Theta_r(s) - \Theta^*(s))$$

This model will be valid if the phase locked loop is in lock or is close to lock.

3.2.2 The Voltage Controlled Oscillator

The voltage controlled oscillator has a linear frequency versus tuning voltage characteristic. This can be written:

$${}_v(t) = k_v \, v_v(t) \quad ,$$

where k_v is an associated gain and $v_v(t)$ is the tuning voltage.

However, $\omega_v(t) = \frac{d}{dt}\,\theta_v(t)$.

Taking Laplace transforms and assuming zero initial conditions gives:

$$\Omega_v(s) = k_v(V_v(s)) = s\Theta_v(s) \quad ,$$

where s is the Laplacian variable, $\Omega_v(s)$ is the Laplace transform of $\omega_v(t)$, $\Theta_v(s)$ is the Laplace transform of $\theta_v(t)$, and $V_v(s)$ is the Laplace transform of $v_v(t)$. Rewriting gives:

$$\frac{\Theta_v(s)}{V_v(s)} = \frac{k_v}{s} \quad .$$

3.2.3 The Loop Filter

The filter immediately following the phase comparator will be designated a transfer function F(s).

3.2.4 The ÷N Counter

The ÷N counter divides the output frequency by a factor

of 2N. Phase is also divided by this factor. Thus, the counter can be represented as a gain of 1/2N.

3.2.5 The Mixer

The mixer mixes the output of the voltage controlled oscillator with the output of the local oscillator. Let the output of the voltage controlled oscillator be given by $\sin(\omega_V t + \theta_V)$ and the output of the local oscillator by $\cos(\omega_L t + \theta_L)$, where ω_L is the local oscillator angular frequency and θ_L is the respective phase. Amplitude information is not relevant,so it will be ignored. The mixer output, y(t), is given by:

$$y(t) = \left[\sin(\omega_V t + \theta_V)\right] \cdot \left[\cos(\omega_L t + \theta_L)\right] .$$

This expression expands to give:

$$y(t) = \sin(\omega_V t + \theta_V + \omega_L t + \theta_L) + \sin(\omega_V t + \theta_V - \omega_L t - \theta) .$$

The sum frequency is filtered out. This leaves only the difference frequency. If the output is given as $\sin(\omega_o t + \theta_o)$, then:

$$\sin(\omega_o t + \theta) = \sin\left[(\omega_V - \omega_L)t + (\theta_V - \theta_L)\right] .$$

This gives the total phase relation:

$$\theta_o(t) = \theta_V(t) - \theta_L(t) .$$

Laplace transforming the above equation and assuming zero initial conditions gives:

$$\Theta_o(s) = \Theta_V(s) - \Theta_L(s) ,$$

where $\Theta_o(s)$ is the Laplace transform of $\theta_o(t)$, $\Theta_V(s)$ is the Laplace transform of $\theta_V(t)$, and $\Theta_L(s)$ is the Laplace transform of $\theta_L(t)$.

Consequently, the mixer can be represented as a summing junction with a gain of 1. This model is shown in Figure 3.2.

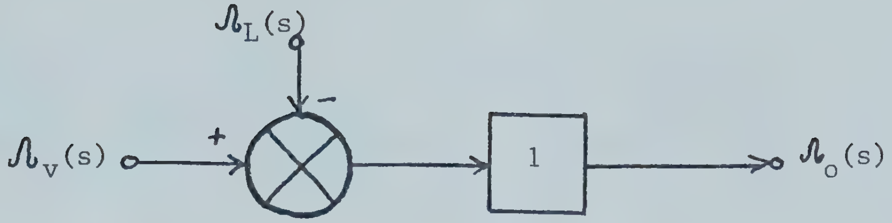


Figure 3.2 Mixer Model

3.2.6 Schmitt Triggers

These circuits do not change the phase information but operate only on the amplitude of the signals. Consequently, their effect can be ignored.

3.3 System Modelling

By replacing the functional blocks in Figure 2.6 with the appropriate models, Figure 3.3 is obtained.

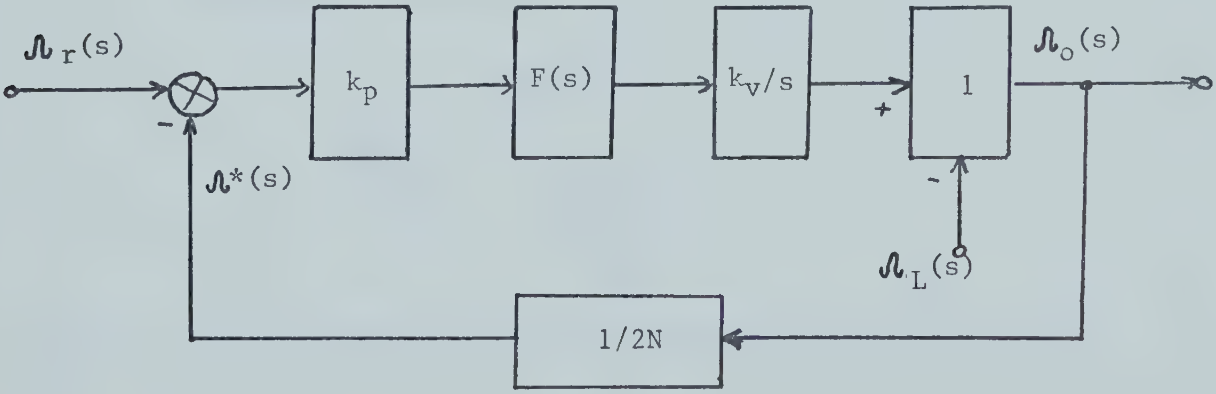


Figure 3.3 System Model

The above model is difficult to analyse. However, the model can be simplified to the equivalent model shown in Figure 3.4.

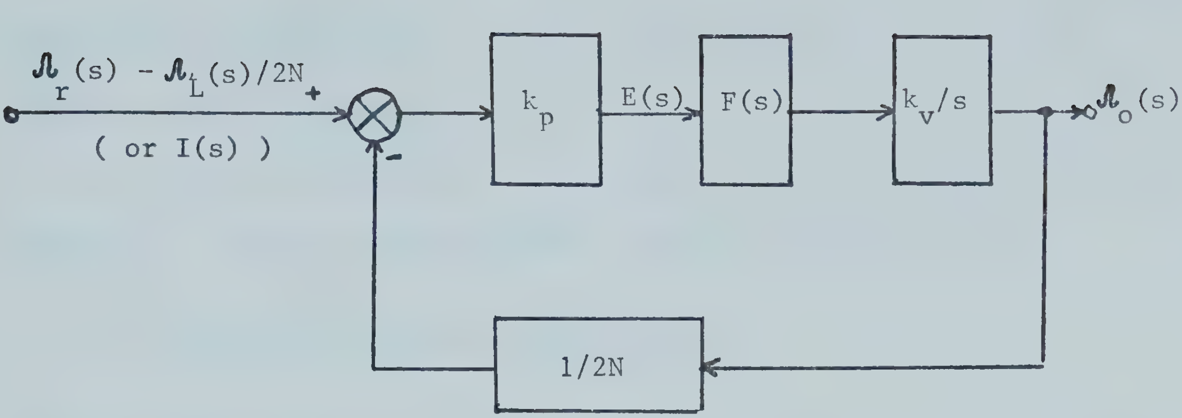


Figure 3.4 Equivalent Model

Let $I(s) = \Theta_r(s) - \Theta_L(s)/2N$. An input to the system occurs when the programming of the ÷N counter is changed. This disturbance can be considered as a change in the input signal, I(s).[5] The system is treated as if the disturbance had arisen by a change in I(s).

A transfer function can now be written. This is:

$$\frac{\vartheta_o(s)}{I(s)} = \frac{\dfrac{k_p k_v F(s)}{s}}{1 + \dfrac{k_p k_v F(s)}{2Ns}} \quad .$$

If F(s) is of the form $k_f(s + a)/s$, then the transfer function becomes:

$$\frac{\vartheta_o(s)}{I(s)} = \frac{k_p k_v k_f (s + a)}{s^2 + (k_p k_v k_f/2N)s + (k_p k_v k_f/2N)a}$$

This equation is of the form:

$$\frac{\vartheta_o(s)}{I(s)} = \frac{K^* (s + a)}{s^2 + 2\zeta_n s + \omega_n^2} ,$$

where K* is a lumped gain,   is the damping ratio, and ${}_n$ is the undamped natural frequency.

A root locus plot of the transfer function is drawn in Figure 3.5. The open loop transfer function is given by:

open

$$\text{open loop function} = \frac{k_p k_v k_f (s + a)}{2Ns^2} \; .$$

The root locus plot is constructed with the pa-ameter $k_p k_v k_f / 2N$ being varied.

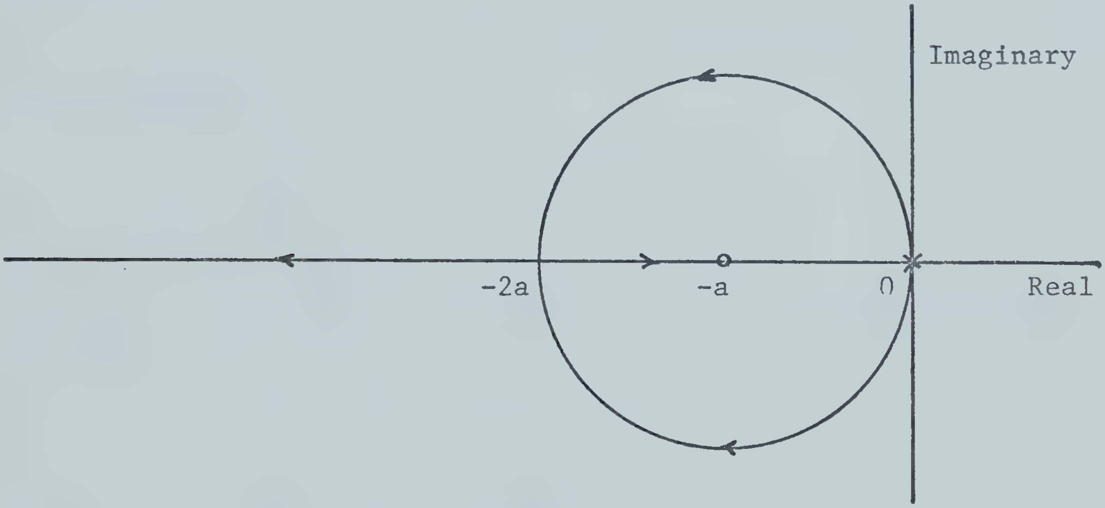


Figure 3.5   Root Locus Plot

The root locus has two branches beginning at the origin, with one asymptote located at 180 degrees. The center of gravity is at s = -a; however, with only one asymptote, there is no intersection at this point. The root locus lies on a circle centered at s = -a, and continues on all portions of the negative real axis to the left of the zero (at s = -a). The breakaway point is at s = -2a. It is evident that the system is unconditionally stable.

3.4 Performance Constants

It is useful to determine the system response to various inputs. The error signal, e(t), is the output of the phase comparator. A transfer function which relates the error signal and the input signal can be found. This is:

$$M(s) = \frac{E(s)}{I(s)} = \frac{k_p s^2}{s^2 + k_p k_v k_f (s + a)/2N} ,$$

where E(s) is the Laplace transform of e(t).

In general, the final value theorem of Laplace transform theory states that:

$$\lim_{t \to \infty} x(t) = \lim_{s \to 0} sX(s) ,$$

where X(s) is the Laplace transform of x(t).

Therefore, the steady/state error of the system can be found by:

$$\text{S.S. error} = \lim_{t \to \infty} e(t)$$

or:

$$\text{S.S. error} = \lim_{s \to 0} sE(s)$$

or:

$$\text{S.S. error} = \lim_{s \to 0} sM(s)I(s) .$$

If the input signal consists of a step in phase, then $I(s) = \Delta\theta/s$, where $\Delta\theta$ is the magnitude of the phase step. For this case:

$$\lim_{s \to 0} sM(s)(\Delta\theta/s) = 0 .$$

The system will completely correct itself for a step in phase. For a frequency step of magnitude $\Delta\omega$, $I(s) = \Delta\omega/s^2$. For this case:

$$\lim_{s \to 0} sM(s)(\Delta\omega/s^2) = \text{S.S. error} ,$$

or:

$$\text{S.S. error} = \lim_{s \to 0} (s) \left[\frac{k_p s^2}{s^2 + k_p k_v k_f (s + a)/2N} \right] \left[\frac{\Delta\omega}{s^2} \right] .$$

This equation implies that the error will be zero. This will be true only if a perfect integrator is used as part of the filter F(s). This is not the case. An operational amplifier was used. In this case, the transfer function is only approximated by F(s). The true filter response is given as (refer to Appendix B):

$$F(s) = A_{OL} \frac{sCR_2 + 1}{sCR_2 + sCR_1 - A_{OL} sCR_1 + 1} ,$$

where R_1, R_2, and C are the component values of the filter, and A_{OL} is the open loop gain of the operational amplifier.

Using this result gives:

$$\text{S.S. error} = \frac{2N(\Delta\omega)}{k_v A_{OL}} .$$

This error is not zero, but is vanishingly small. Thus, the system will track out a step in frequency.

3.5 Loop Parameters

The loop transfer function was previously given as:

$$\frac{\Omega_o(s)}{I(s)} = \frac{k_p k_v k_f (s + a)}{s^2 + (k_p k_v k_f/2N)s + (k_p k_v k_f/2N)a} .$$

This equation is of the form:

$$\frac{\Omega_o(s)}{I(s)} = \frac{K^*(s + a)}{(s^2 + 2\zeta_n s + \omega_n^2)} .$$

Therefore:

$$\omega_n = \sqrt{\frac{k_p k_v k_f \ a}{2N}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{k_p k_v k_f}{2aN}}$$

In this system, N varies from 1 to 200. For a nominal design, N was selected to be the geometric mean of the two extremes. This gives $N = \sqrt{200}$. A value of N = 14 was used. For this value of N, a damping ratio of ½ was chosen. Also for this value of N, the output frequency error was to be less than 10% for a time greater than 0.1 second. From normalized curves[7], it is found that the output error will be less than 10% with $\zeta = \frac{1}{2}$, for $\omega_n t$ greater than 4. Therefore:

$$\omega_n \geq \frac{4}{t}$$

Let $\omega_n = 40$. This gives:

$$40 = \sqrt{\frac{k_p k_v k_f}{28}}$$

Also, from the damping ratio relationship:

$$\tfrac{1}{2} = \tfrac{1}{2}\sqrt{\frac{k_p k_v k_f}{28\,a}}$$

These equations yield:

$$a = 40$$

and $$k_p k_v k_f = 1120$$

The values of ω_n and ζ will vary with N. Table 3.1 gives

the values of ω_n and ξ as functions of N. The settling time (time to reach 10% error) is also given. The settling time is found from normalized curves.[7]

N	ω_n	ξ	Settling Time	$\omega_n t$ for $<10\%$ error
1	149.6	1.875	0.004 (sec)	0.6
4	74.8	0.938	0.043	3.2
14	40.0	0.50	0.10	4.0
50	21.6	0.265	0.416	9.0
200	10.6	0.133	1.25	13.3

Table 3.1 Values of ω_n and ξ

The values of a and k_f are determined by the values of the components comprising the loop filter (refer to Appendix B). To satisfy the requirements put forth for ω_n and ξ, 'a' must be equal to 40 and $k_p k_v k_f$ must be equal to 1120. The value of k_p was found in Chapter 5, section 1. A value k_v' was also found in Chapter 5, section 1. The value of k_v' is the sensitivity of the voltage controlled oscillator to the coarse tuning voltage. The voltage controlled oscillator does not require this large value of sensitivity for the input from the phase comparator/loop filter. An order of magnitude reduction is possible. A value of $k_v = k_v'/10$ is used for the voltage controlled oscillator sensitivity for this input. This gives:

$$k_v = 1.05 \times 10^3$$

$$k_p = 23.2$$

Therefore: $k_f = 0.046$

The loop filter component values can now be calculated. The two necessary relations are:

$$a = 1/R_2C = 40$$

$$k_f = R_2/R_1 = 0.046$$

If C is chosen to be 6.8 μf, then:

$$R_2 = 3.68 \text{ k} \approx 3.9 \text{ k}$$

$$R_1 = 84.8 \text{ k} \approx 82 \text{ k}$$

CHAPTER 4

CIRCUIT DETAILS

4.1 Introduction

Several of the circuits used in the tone burst generator are of a novel design. These circuits are presented in this chapter. The circuits that are of a more standard nature are presented in Appendix C.

4.2 The ÷N Counter

This counter is a three decade down counter. The desired value of N is programmed into the counter in a binary coded decimal (BCD) form. The programming is obtained either from BCD output thumbwheel switches or from an external source. The counter counts down from its programmed value until zero is reached. This condition is decoded and an output pulse is generated. This pulse reloads the program into the counter and toggles an output flip-flop. The counter is now ready to begin another count cycle. A block diagram of the counter is shown in Figure 4.1.

Each decade of the counter was constructed as a synchronous counter using integrated circuit logic gates and flip-flops. The flip-flops used do not have a "set" capability but do have a "reset" capability. Here "reset" means "set to zero". Consequently, the counting sequence is that which would normally be termed "up counting". The logic states are shown in Table 4.1. The letters A, B, C, and D refer to the bits of the decade counter where A is the most significant bit and D is the least significant bit.

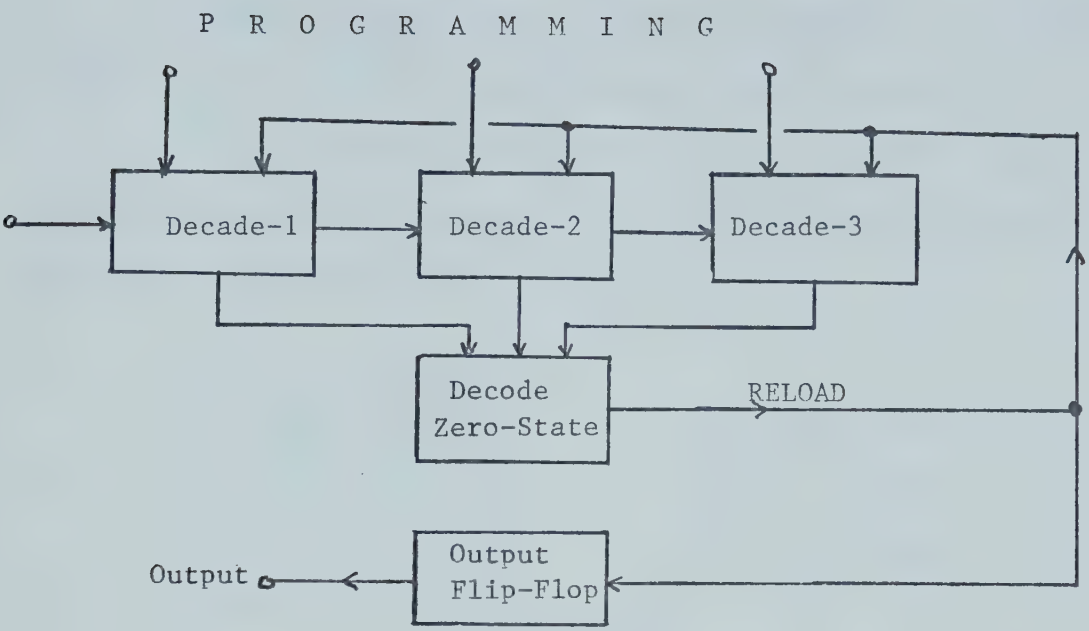


Figure 4.1 Block Diagram of the ÷N Counter

Corresponding Numeral	A	B	C	D
9	0	1	1	0
8	0	1	1	1
7	1	0	0	0
6	1	0	0	1
5	1	0	1	0
4	1	0	1	1
3	1	1	0	0
2	1	1	0	1
1	1	1	1	0
0	1	1	1	1

Table 4.1 Counting Sequence

This counting scheme allows the programming to be loaded into the counter by resetting the appropriate flip-flops.

The flip-flops used are J-K flip-flops. The J and K inputs have been tied together. Table 4.2 shows the flip-flop response for this situation.

J/K	Q_n	Q_{n+1}
1	X	X
0	X	$\overline{X}$

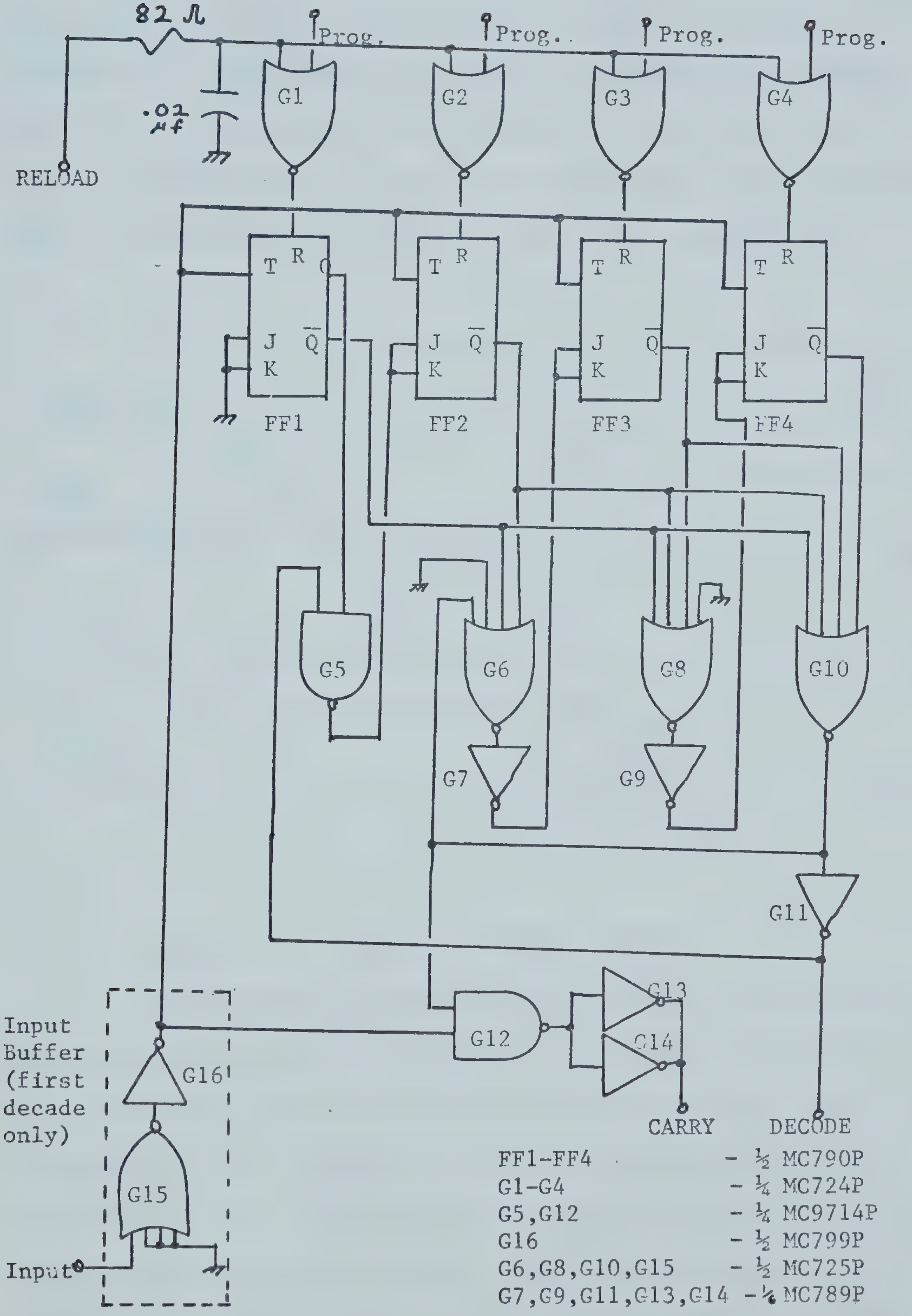
X is a don't care

Q_{n+1} is Q_n after one clock pulse

Table 4.2 Flip-Flop Response

An individual flip-flop will change states at a clock pulse if its J/K inputs are low, that is, zero. It will not change states if its J/K inputs are high. The counter functions by decoding the state of the counter,and using the decoded outputs to program the J/K inputs of the flip-flops. A schematic diagram of one decade of the counter is shown in Figure 4.2.

Logic gates G5, G6, G8, and G10 perform the decoding function. These gates provide the required J/K programming as well as decoding the decade zero state. Logic gates G12, G13, and G14 produce a "CARRY" pulse. Gate G12 is enabled when the decade is in the zero state. Consequently, the next clock pulse will be passed to the next decade. This method relies upon gate delays at certain times. If the decade of interest contains the equivalent of the numeral zero(that is, 1111), and the next decade contains the equivalent of the numeral one (that is 1110),then the



FF1-FF4 - ½ MC790P
G1-G4 - ¼ MC724P
G5,G12 - ¼ MC9714P
G16 - ½ MC799P
G6,G8,G10,G15 - ½ MC725P
G7,G9,G11,G13,G14 - ⅙ MC789P

Figure 4.2 Schematic of One Decade of the ÷N Counter

next clock pulse advances both decades. However the decade of interest will change from 0 to 9 before the second decade changes from 1 to 0. Consequently, the condition of both decades being in the zero state does not occur and a false reset cycle is avoided. This is illustrated in the timing diagram shown in Figure 4.3.

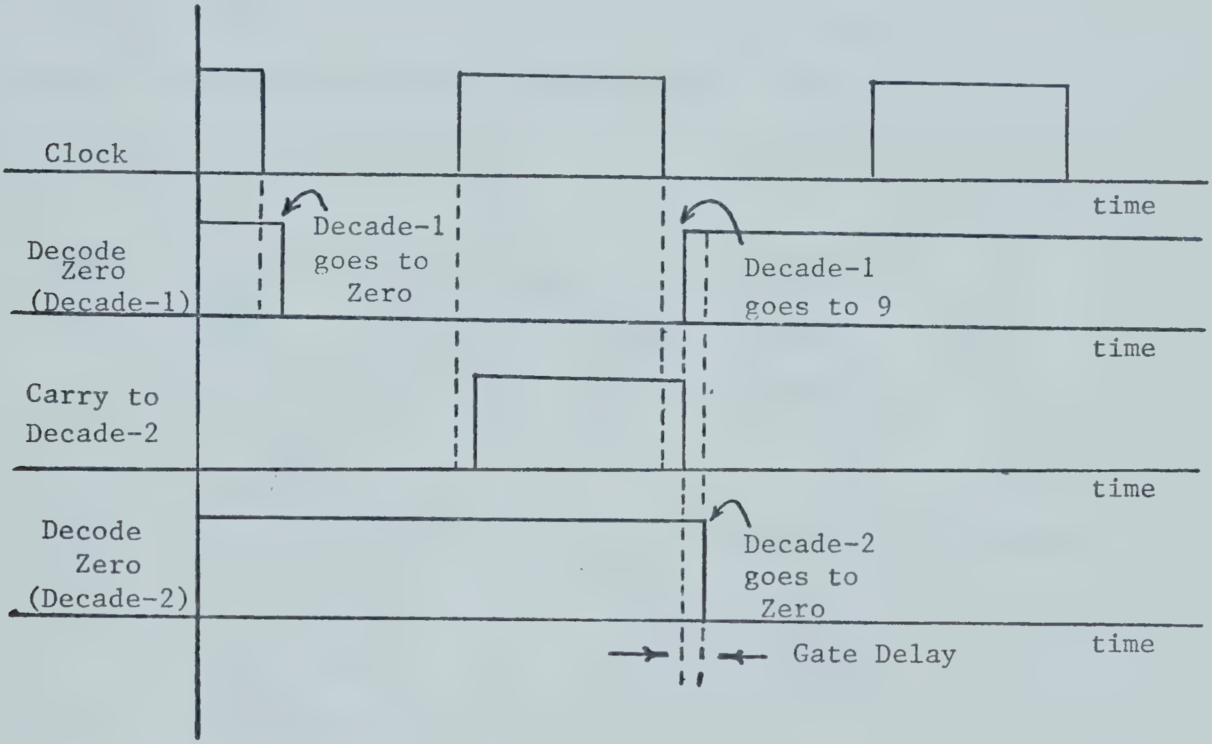


Figure 4.3 Carry Pulse Timing Diagram

The program is loaded into the counter by resetting or not resetting the particular flip-flop concerned. That is, if a 1 is required in a particular flip-flop, that flip-flop is not reset; but if a 0 is needed, then that flip-flop is reset. The reset inputs of the flip-flops are driven by NOR gates. The RELOAD input to each gate (G1 - G4) holds the gate outputs low. This condition has no effect on the flip-flops. When the counter has reached the zero state, the RELOAD bus goes low. The programming

inputs now determine which flip-flops are reset. This allows the program to be loaded into the counter. The program must be the complement of normal BCD to achieve correct programming.

Each decade decodes its own zero state. The decoded outputs from each decade are fed to an additional decoder. This circuit determines when the entire counter has reached the zero state, not merely one decade of the counter. This circuit is shown in Figure 4.4.

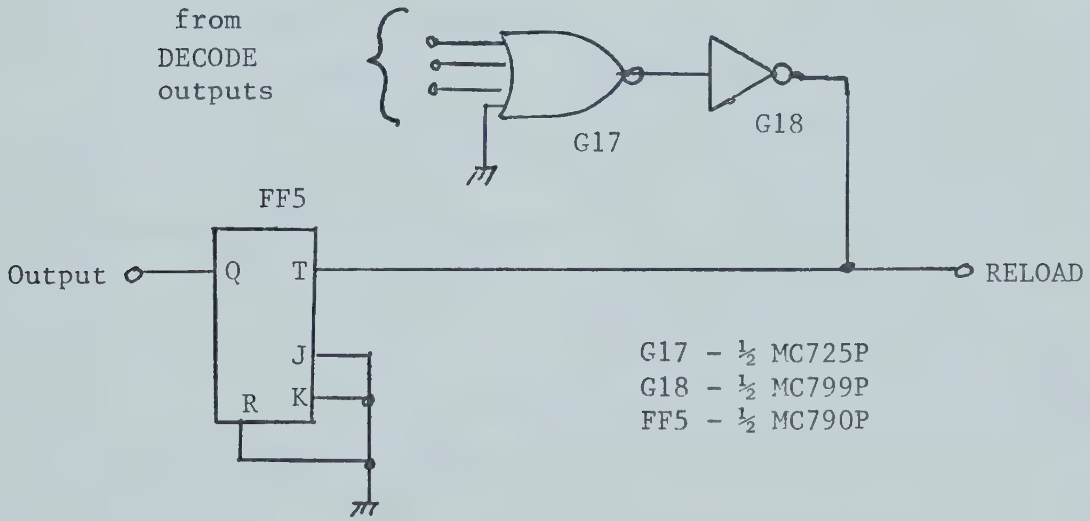


Figure 4.4 ÷N Decoder Circuit

The RELOAD signal is a pulse, since as soon as the program has entered into the counter, the decode circuit will no longer see the counter in the zero state. The RELOAD pulse will have a width of only several gate delays. This pulse occurs once every N clock pulses, where N is the number programmed into the counter. The RELOAD pulse toggles an output flip-flop (FF5) to give an output square wave with frequency equal to the input frequency divided by 2N.

4.2 Rise/Fall Counter

This counter consists of a three decade down counter, and its design was similar to that of the ÷N counter. Only the decoding of the zero state, the input buffer, and the last (most significant) decade vary. A schematic diagram of this part of the counter is given in Figure 4.5.

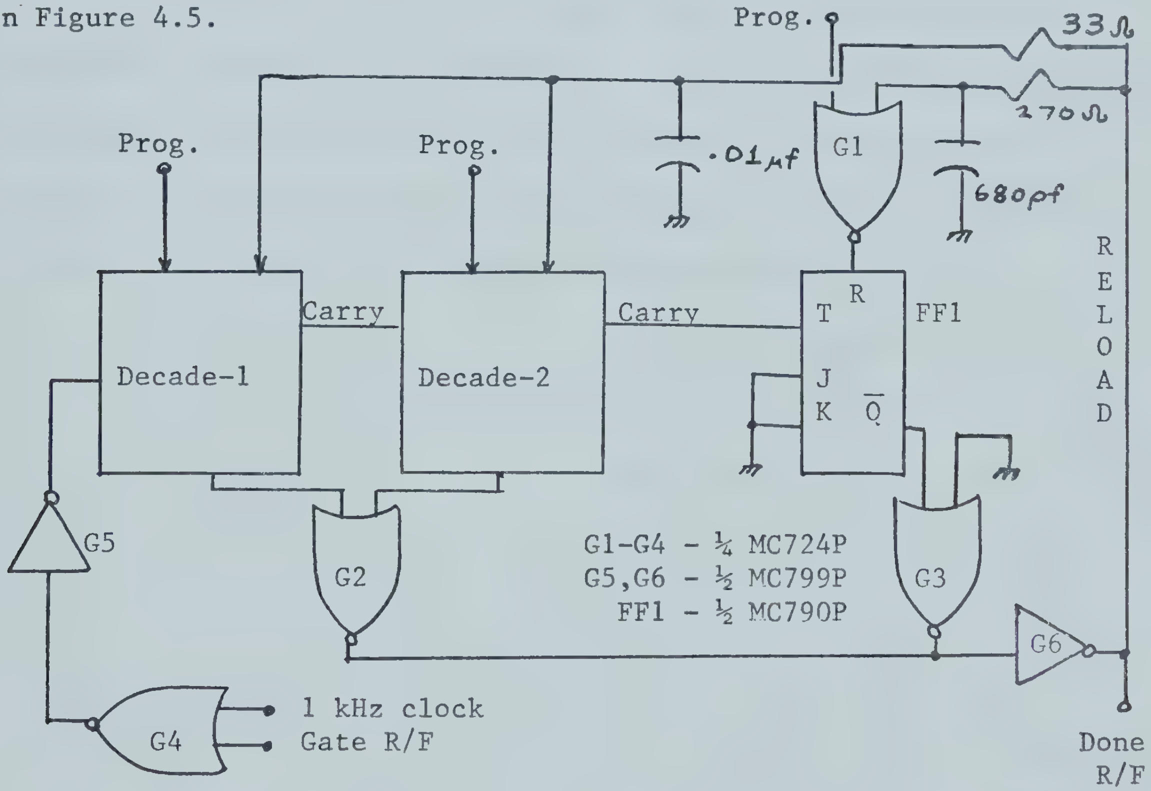


Figure 4.5 Schematic of the Rise/Fall Counter

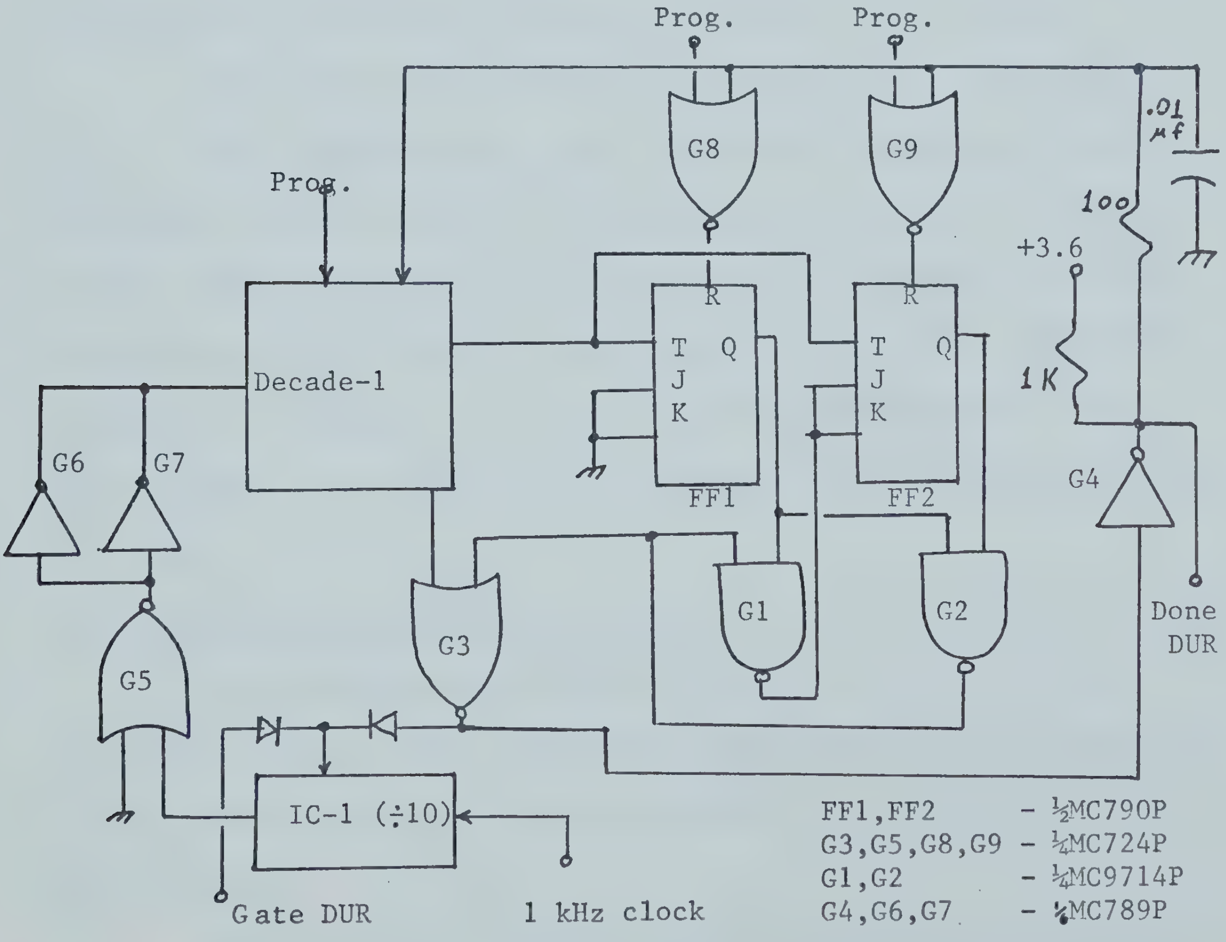
The last decade of this counter can assume only two values, either a 1 or a 0. Consequently, the largest number which can be programmed into the counter is 199. Therefore, the longest trapezoid rise/fall time which can be produced is 199 milliseconds.

Gate G4 is fed the 1 kHz clock signal and the GATE R/F signal from the trapezoid controller circuit. The GATE R/F signal is normall- high, Thus preventing the 1 kHz signal from toggling

the counter. When a trapezoid is to be generated, the GATE R/F signal will go low and allow the 1 kHz clock signal to toggle the counter. The RELOAD signal is fed back to the trapezoid controller. This signal is the R/F DONE signal shown in Figure 2.8.

4.3 The Duration Counter

This counter is a two decade down counter, and its design was similar to that of the ÷N counter. The first decade of the counter is identical to the decades of the ÷N counter. The last decade, the counter zero state decoding, and the input buffer are different. A schematic diagram of the counter is given in Figure 4.6.



FF1,FF2 - ½MC790P
G3,G5,G8,G9 - ¼MC724P
G1,G2 - ¼MC9714P
G4,G6,G7 - ¼MC789P

Figure 4.6 Schematic of the Duration Counter

Gates G1 and G2 perform the necessary decoding and program the J/K inputs of FF1 and FF2. Gate G3 decodes the counter zero state. The 1 kHz clock input is divided down to 100 Hz by the integrated circuit decade counter IC1. The reset terminal of IC1 is fed from the trapezoid controller circuit and is used to gate the counter on and off. The RELOAD pulse is fed back to the trapezoid controller. This pulse is the DUR DONE signal shown in Figure 2.8.

4.5 The Phase Comparator and Loop Filter

A schematic diagram of the phase comparator is shown in Figure 4.7. The loop filter is also shown in this figure.

The actual phase comparison is made by IC1. Transistors Q1 and Q2 are amplifiers that boost the level of the input signals. The output of IC1 consists of a differential pulse width modulated signal. Operational amplifier IC2 converts this signal to a single ended output of both positive and negative going pulses. Operational amplifier IC3 comprises the loop filter and integrates the pulses to a DC level. The values of R_1, R_2, and C were calculated in Chapter 3, section 5.

4.6 The Voltage Controlled Oscillator

The voltage controlled oscillator must be tunable over a specified frequency range. The output amplitude must be independent of the output frequency. A block diagram of the oscillator is shown in Figure 4.8.

The two current sources alternately charge and discharge

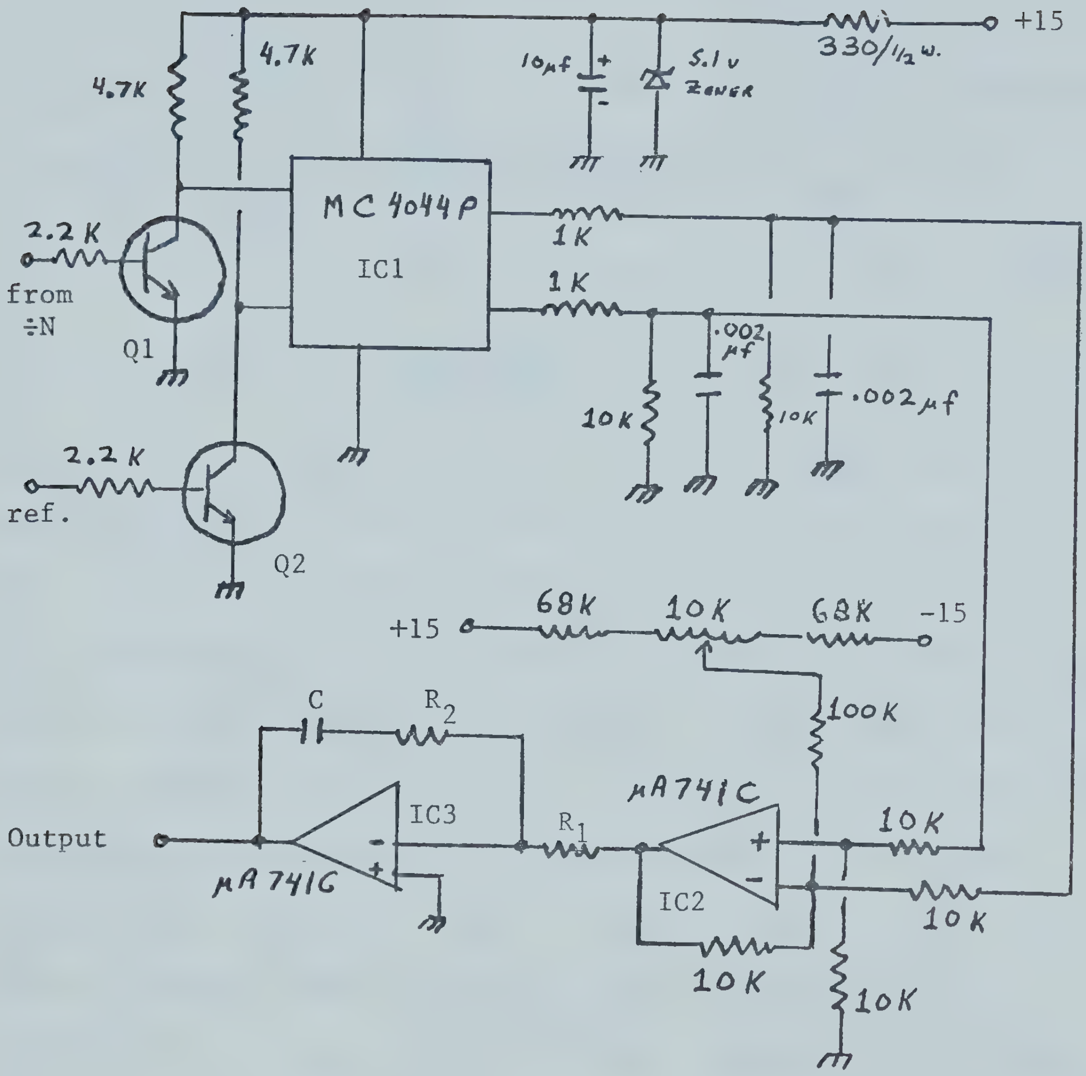


Figure 4.7 Schematic of the Phase Comparator & Loop Filter

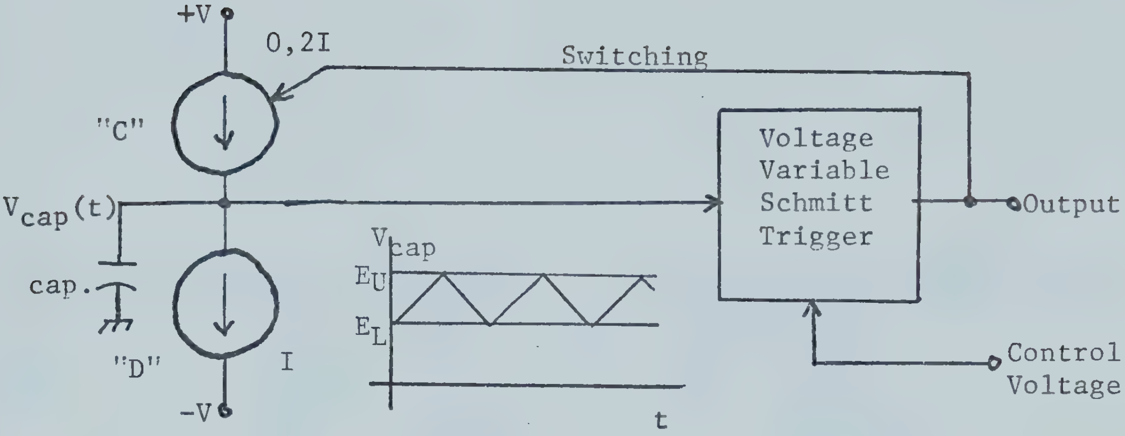


Figure 4.8 Block diagram of the Voltage Controlled Oscillator

the capacitor. Current source D is fixed at a value of I. Current source C is switched between the values of 0 and 2I. When C is off, a net current of I will discharge the capacitor. When C is on, a net current of I will charge the capacitor. The Schmitt trigger has an upper trigger level of E_U and a lower trigger level of E_L. These two values are not the same. Consequently, when C is off the voltage across the capacitor will decrease until E_L is reached. This voltage switches the Schmitt trigger. C will be turned on and the voltage across the capacitor will increase until E_U is reached. This voltage causes the Schmitt trigger to switch again. The input to the Schmitt trigger will be a triangular waveform with upper and lower values of E_U and E_L, respectively. The Schmitt trigger output will be a square wave. The control voltage varies the lower trigger point of the Schmitt trigger.[6] The value of E_L affects the period of the triangular waveform and therefore the output frequency. A schematic diagram of the voltage controlled oscillator is given in Figure 4.9.

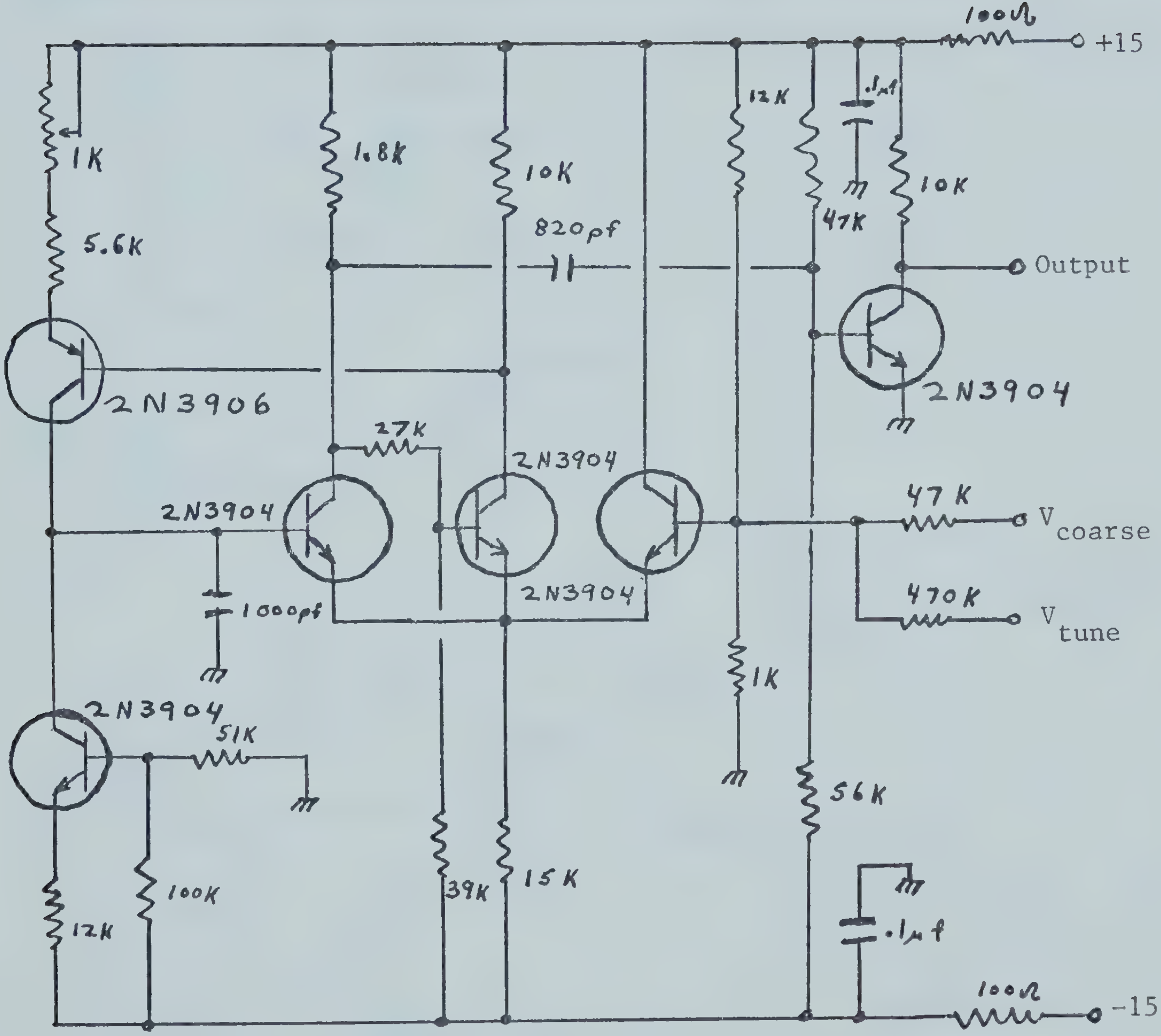


Figure 4.9 Schematic Diagram of the Voltage Controlled Oscillator

4.7 The Trapezoid Synthesizer and Gain Control Circuit

This circuit actually produces the trapezoidal waveform. It is controlled by the trapezoid controller circuit. A schematic diagram of this circuit is shown in Figure 4.10.

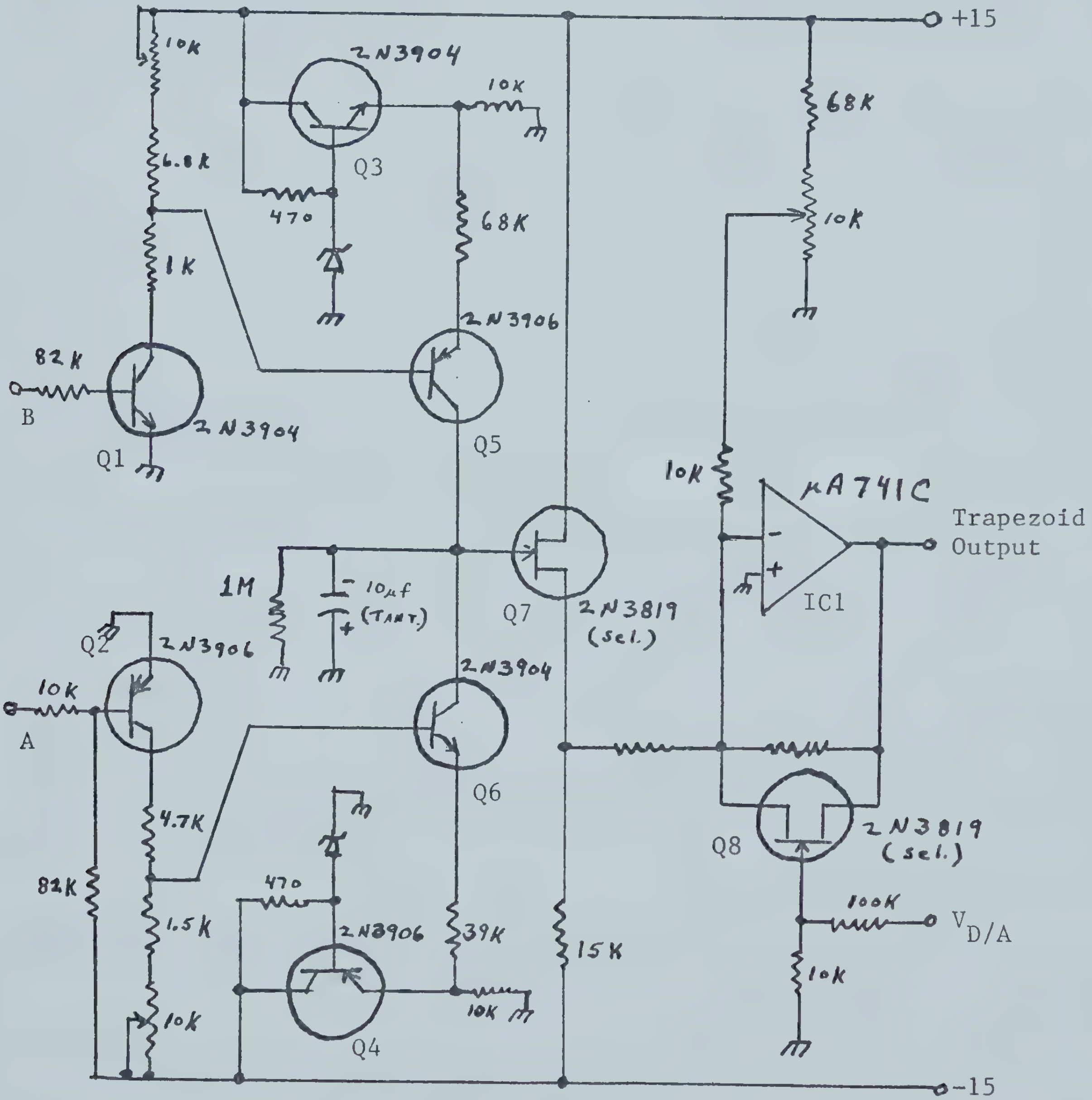


Figure 4.10 Schematic Diagram of the Trapezoid Synthesizer & Gain Control Circuit

Transistors Q5 and Q6 comprise the two current sources that charge and discharge the capacitor C1. Transistors Q1 and Q2 accept the A and B inputs from the trapezoid controller. These transistors switch Q5 and Q6 on and off. Transistors Q3 and Q4 drop the power supply voltage to ±10 volts, thus enabling Q5 and Q6 to be switched off.

Transistor Q7 buffers the trapezoid waveform to the gain control circuit. The gain control circuit consists of Q8 and IC1. The voltage dependent drain-to-source resistance of Q8 (an FET) is used to vary the gain of the operational amplifier. The gain is determined by the control voltage, $V_{D/A}$, which is obtained from the Rise/Fall digital to analog converter.

4.8 The Trapezoid Controller

The trapezoid controller generates the switching sequence required to synthesize a trapezoid. The required switching functions are illustrated in Figure 4.11. The circuit was built up using integrated circuit logic gates and flip-flops to obtain the required control logic. A schematic diagram of this circuit is shown in Figure 4.12.

4.9 The Trigger Circuit

The trigger circuit determines the time at which a trapezoid is initiated. Two conditions must be met before a trapezoid is initiated. First, a trigger pulse must occur; and second, the sinusoid must be at a point of zero phase. A schematic

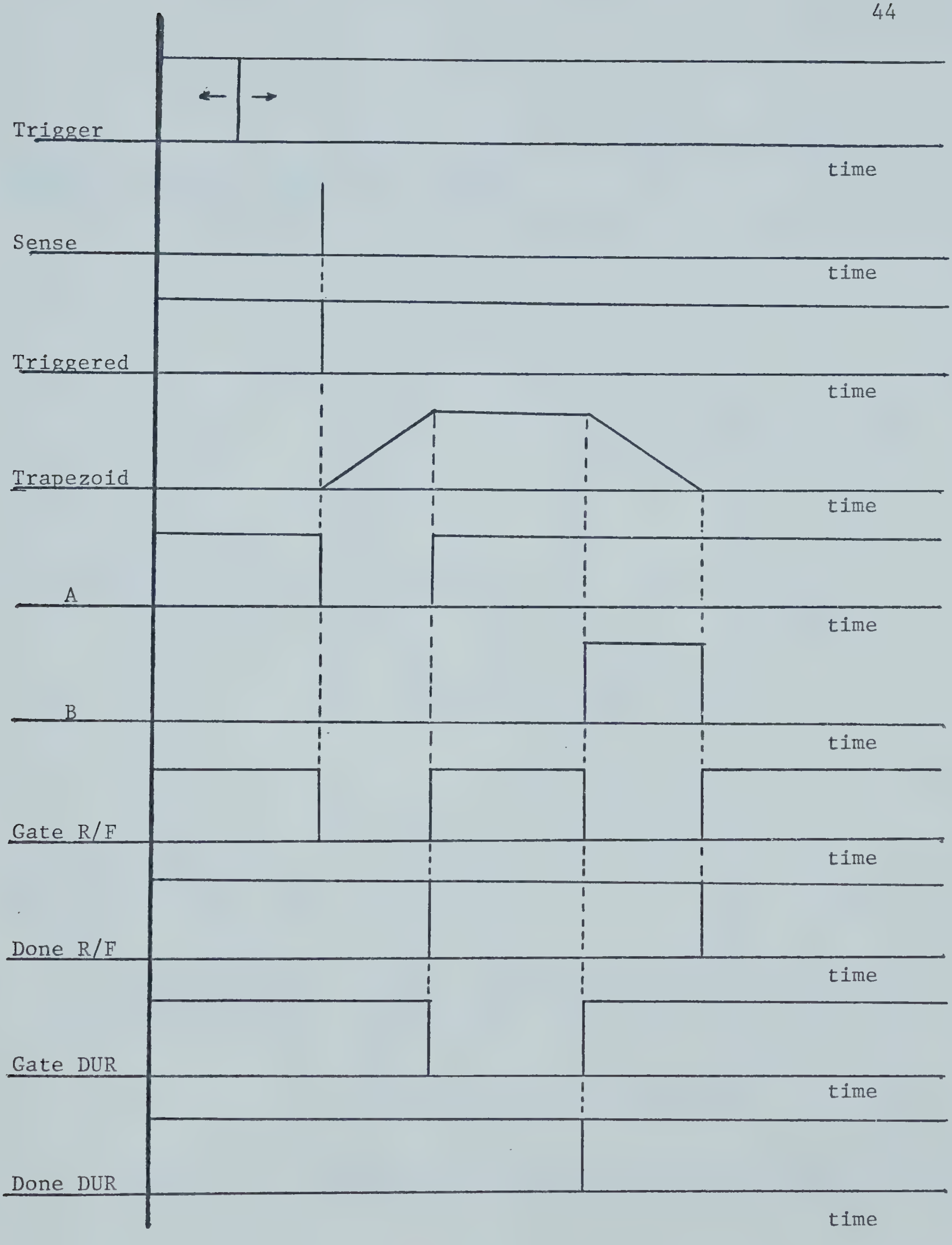


Figure 4.11 Trapezoid Controller Switching Sequence

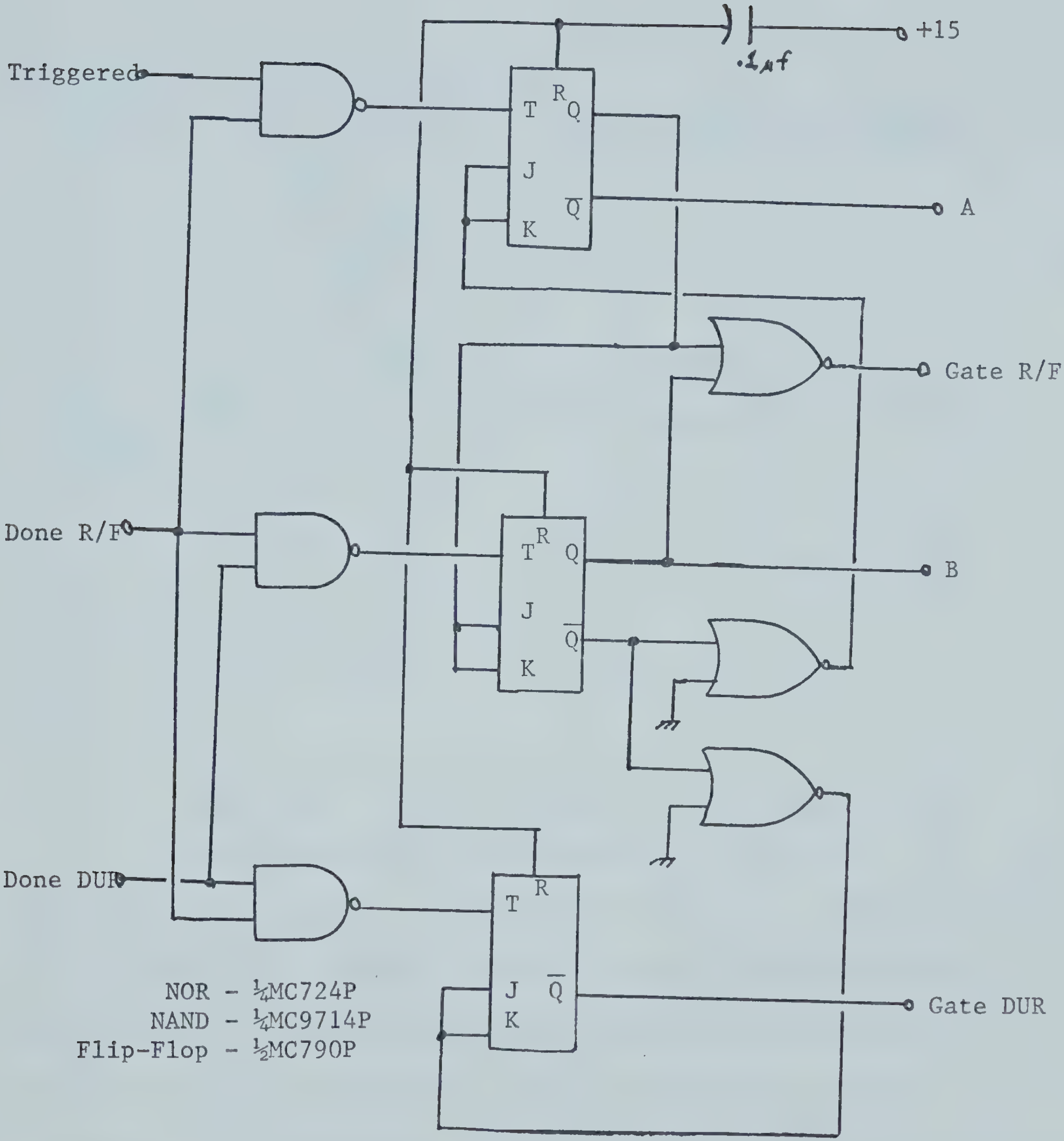


Figure 4.12 Schematic Diagram of the Trapezoid Controller

diagram of this circuit is shown in Figure 4.13.

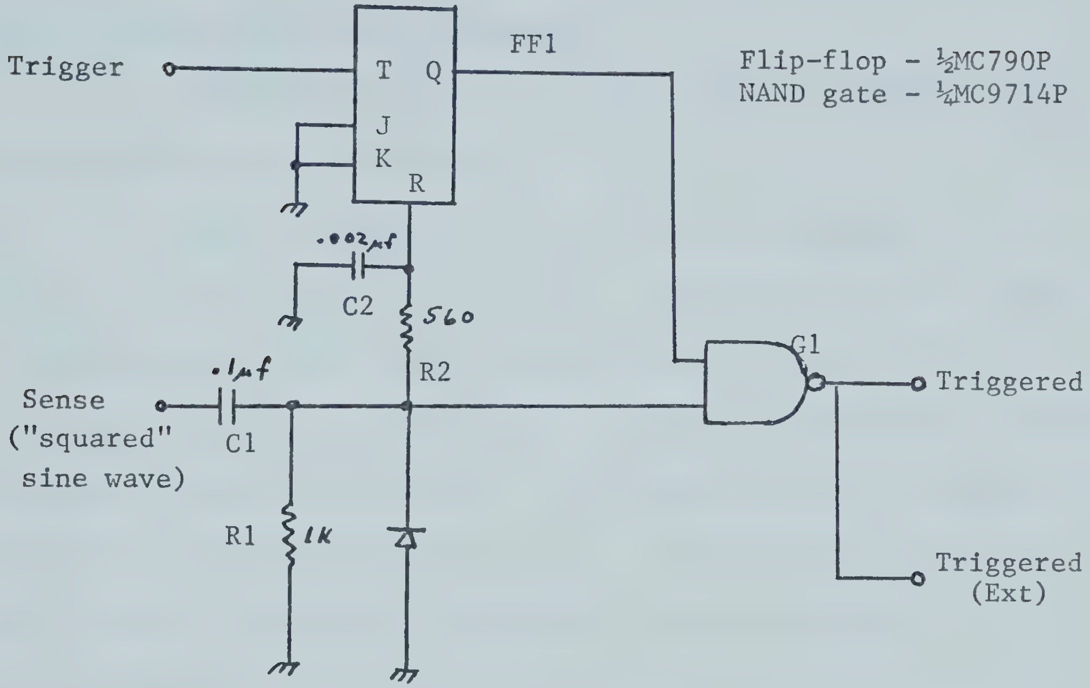


Figure 4.13 Schematic Diagram of the Trigger Circuit

The trigger pulse is detected by flip-flop FF1. The pulse sets the flip-flop. The "squared" sine wave is differentiated by R1 and C1. The resulting "spikes" are fed to the NAND gate G1. When the gate has been enabled by the flip-flop, the next spike will be transmitted through the gate and trigger the trapezoid controller. The spikes are also used to reset the flip-flop. Enough time delay is included (R2 and C2) to ensure that a non-ambiguous pulse is transmitted by the gate.

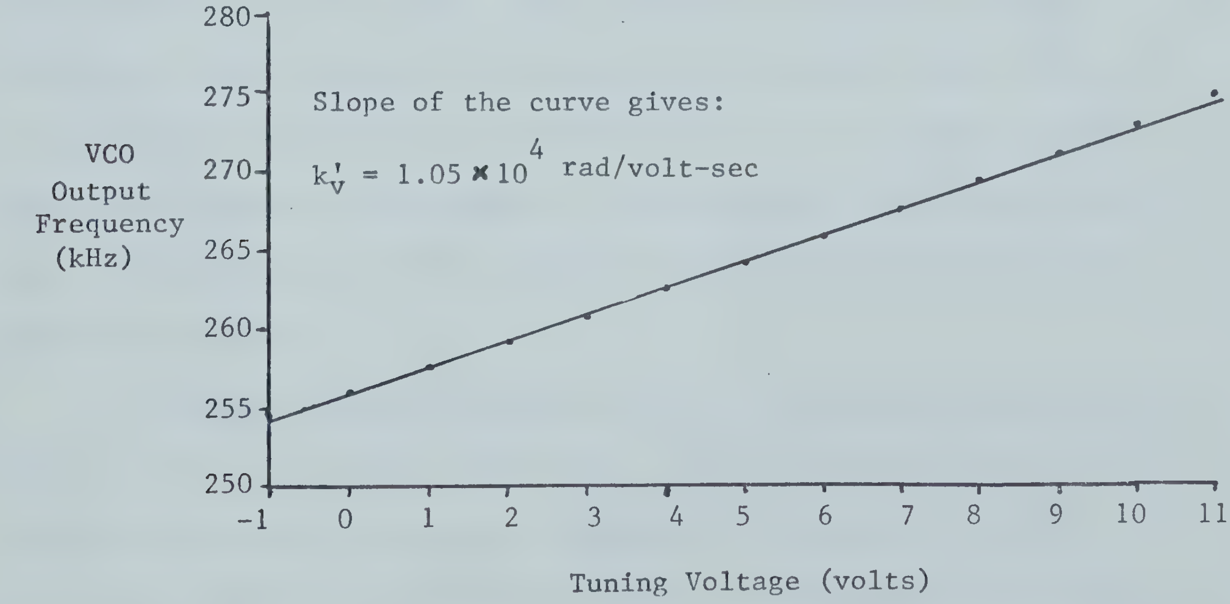
CHAPTER 5

EVALUATION OF THE SYSTEM

5.1 Phase Locked Loop Measurements

Several parameters are of importance in evaluating the phase locked loop performance.

First, in Chapter 3, two assumptions were made in the analysis of the phase locked loop. These were that the voltag controlled oscillator output frequency varied linearly with the tuning voltage, and that the phase comparator output varied linearly with the input phase difference. The response of the voltage controlled oscillator was measured and is illustrated in Figure 5.1. The response of the phase comparator is shown in Figure 5.2. It can be seen that the actual responses closely approximate linear responses.



Slope of the curve gives:

$k_v' = 1.05 \times 10^4$ rad/volt-sec

Figure 5.1 The Voltage Controlled Oscillator Response

The slope of the curve in Figure 5.1 gives the value of k_v', the voltage-controlled-oscillator sensitivity constant. The value of this constant gives the oscillator sensitivity to the coarse tuning voltage. The tuning voltage derived from the filter/phase comparator has a much attenuated effect, as discussed in Chapter 3, page 28. The sensitivity to this signal is given by k_v.

The output of the phase comparator was measured by applying a known step in phase to the phase comparator inputs and measuring the slope of the resulting at the loop filter output. Assuming that the zero of the loop filter can be ignored, the output of the filter is given as:

$$v(t) = (k_p)(\Delta \emptyset)(t)(k_f) \quad ,$$

where $\Delta\emptyset$ is the magnitude of the phase step. Thus, the slope of the ramp is $(k_p)(\Delta\emptyset)(k_f)$. If a known value of k_f is temporarily used, the value of k_p can be found. This procedure is necessary as the comparator output consists of a pulse width modulated signal, that is, the comparator output consists of either positive or negative pulses, the width of which is determined by the magnitude of the input phase step. Pulse polarity is determined by the lag/lead relation of the two input signals.

Second, the phase locked loop was to generate fixed amplitude sine waves of various frequencies. Figure 5.3 shows a plot of the power amplifier outputs as a function of frequency. A fixed voltage was applied to the trapezoid input of the modulator to obtain a measurable output.

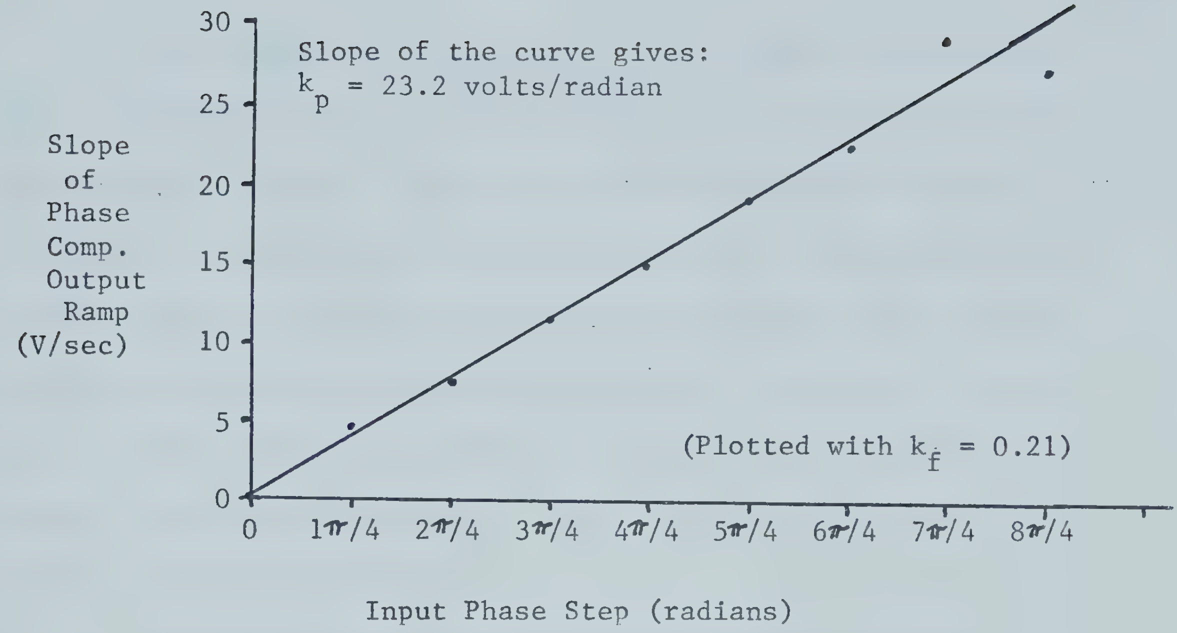


Figure 5.2 The Phase Comparator Response

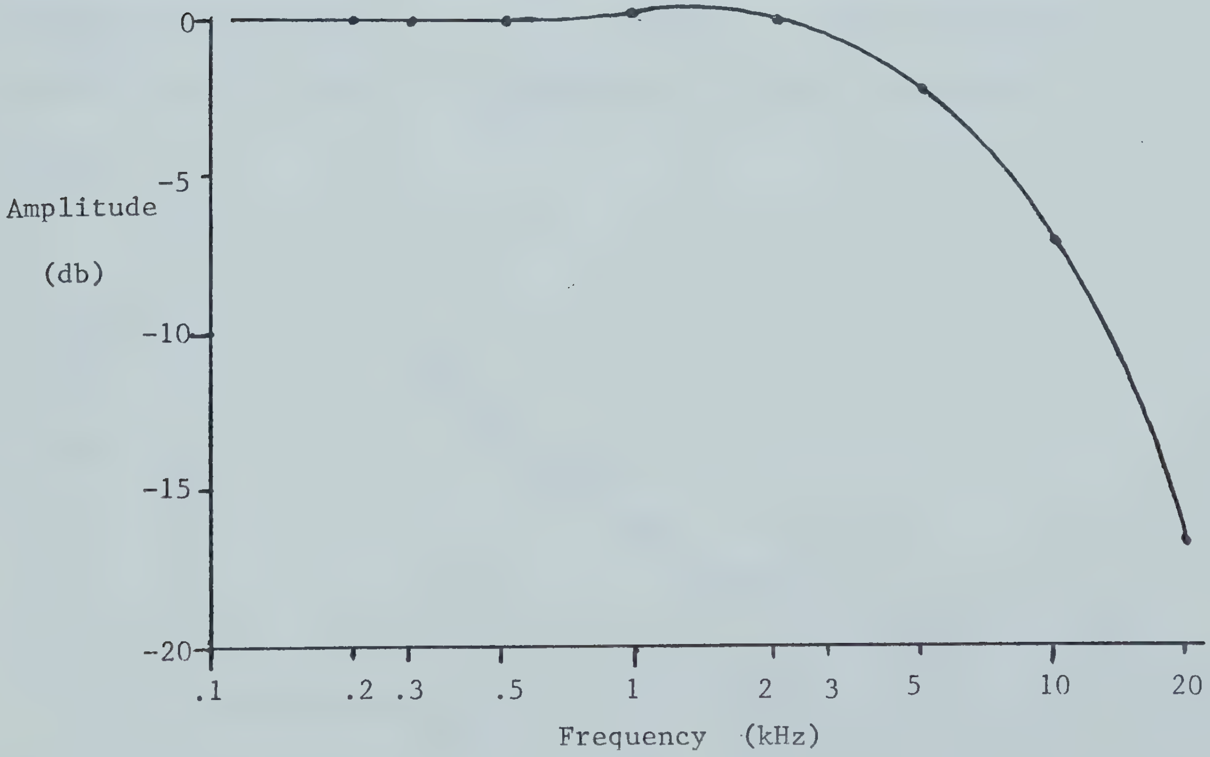


Figure 5.3 Amplitude vs Frequency Response

The frequency response rolls off sooner than expected. This results from the extensive compensation required to prevent spurious oscillations. The integrated circuit multipliers are especially responsible for the rapid roll-off. These circuits required large amounts of compensation to prevent spurious oscillations. The power amplifiers also required compensation to prevent oscillations from occurring. All these factors combine to degrade the frequency response. As a result, the frequency response is 7db down at 10 kHz.

The distortion of the sinusoid was also measured. A plot of the distortion versus frequency is shown in Figure 5.4. A fixed voltage (equal to the peak trapezoid voltage) was applied to the trapezoid input of the multiplier to obtain a measurable output.

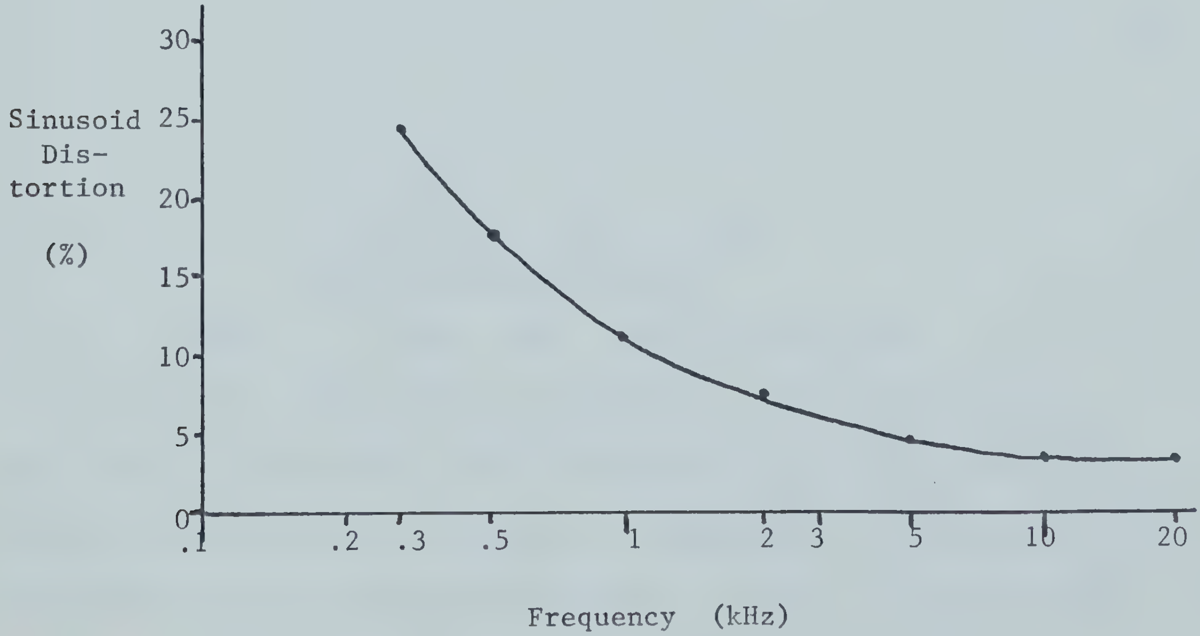


Figure 5.4 Distortion of the Sinusoid

The large values of distortion which were measured are misleading. Any noise in the system causes phase jitter and this jitter contributes to the distortion as measured with a distortion analyser (Hewlett-Packard 330B). The jitter is more pronounced at lower frequencies and thus a larger distortion figure is measured at lower frequencies.

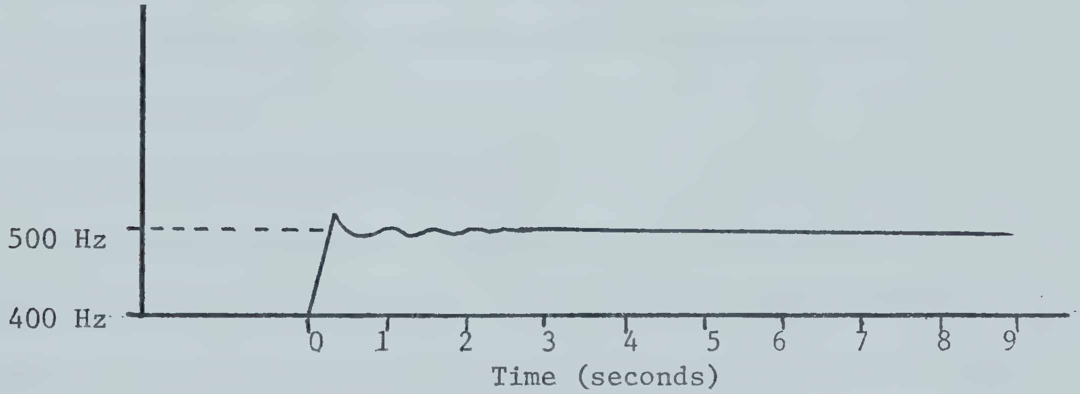
Third, the phase locked loop was to have specified transient response characteristics. That is, the damping ratio, the natural undamped resonant frequency, and the settling times were to be close to the values given in Table 3.1 (page). Only the settling times can be conveniently measured. Table 5.1 shows the settling times which were actually obtained.

N	Settling Time
4-5	0.1 sec
4-14	0.2 "
40-50	0.2 "
10-110	0.6 "
100-200	unavailable

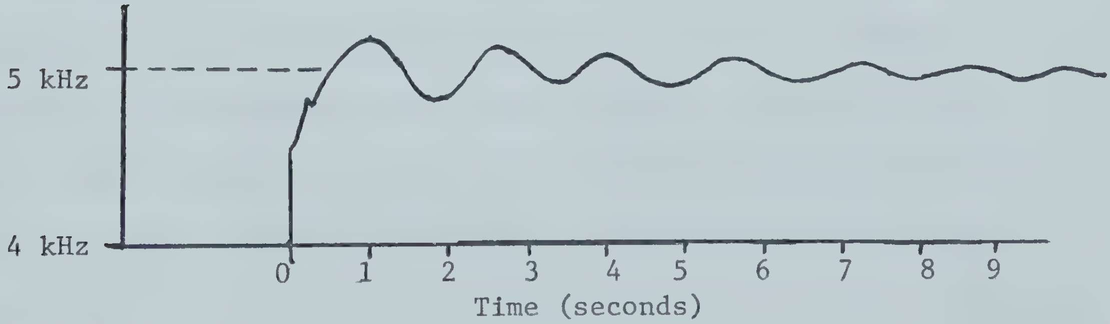
Table 5.1 Phase Locked Loop Settling Times

These values are very reasonable. The settling time for 20 kHz is unavailable since the amplitude of the sine wave rolls off rapidly at this frequency. Consequently, the frequency detecter circuits employed give erroneous results at this frequency.

The response of the system to various steps in N is shown in Figure 5.5. The damped responses are typical of other settings of N. The responses were obtained by setting N at a specified value and dialing a step in frequency, that is, by suddenly dialing a different value of N. The output sinusoid was monitored by the circuits shown in Figure 5.6. The outputs of these circuits were monitored with a storage oscilloscope. The outputs of these circuits are proportional to the input frequency applied to them.

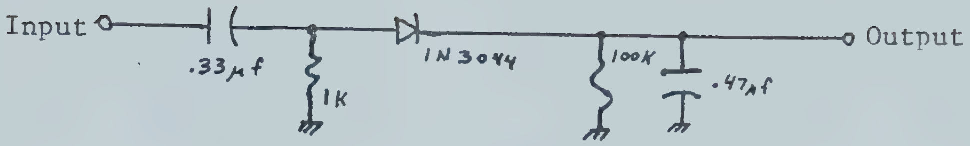


(a) 400 Hz to 500 Hz Response

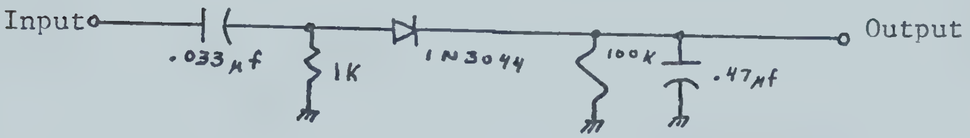


(b) 4 kHz to 5 kHz Response

Figure 5.5 Phase Locked Loop Output Frequency Error Response



(a) 500 Hz to 400 Hz Circuit



(b) 4 kHz to 5 kHz Circuit

Figure 5.6 Frequency Measuring Circuits

The output of the phase locked loop was to consist of a sinusoid of specified frequency. The output contains, however, a small amount of the sum frequency produced by the mixer. This component was measured and was found to be 50 db down from the desired output signal.

5.2 Trapezoid Generator Measurements

Two parameters are of importance in the evaluation of the trapezoid generator's performance. These are the trapezoid droop and the trapezoid peak amplitude as a function of rise/fall times. The trapezoid droop results from leakage currents which discharge the holding capacitor in the Trapezoid Synthesizer circuit. Ideally, the voltage on the capacitor would remain constant for an indefinite length of time. However, leakage currents cause a discharging of the capacitor and hence the resulting droop. This effect is illustrated in Figure 5.7.

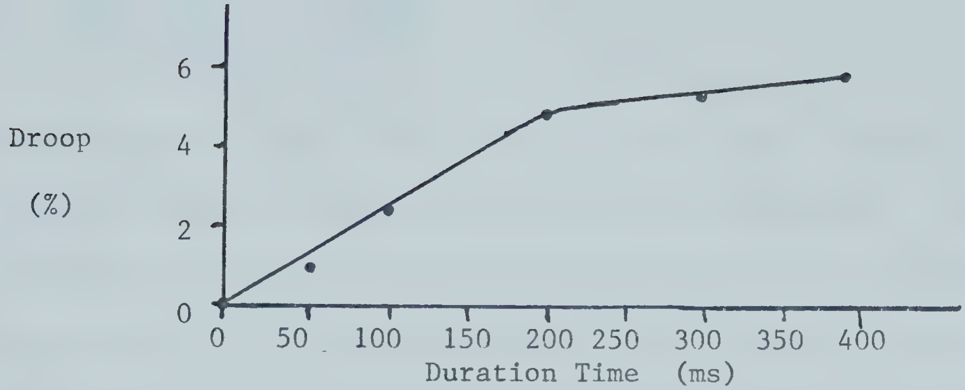


Figure 5.7 Trapezoid Droop

The accuracy of the Gain Control Circuit determines how well the trapezoid generator maintains a constant peak amplitude as the rise/fall times vary. The Trapezoid Synthesizer produces trapezoids with varying peak amplitudes. The Gain Control Circuit is controlled by the output voltage of the Rise/Fall Digital to Analog Converter and either amplifies or attenuates the trapezoid to produce trapezoids of constant peak amplitude. This aspect of the trapezoid generators performance is illustrated in Figure 5.8.

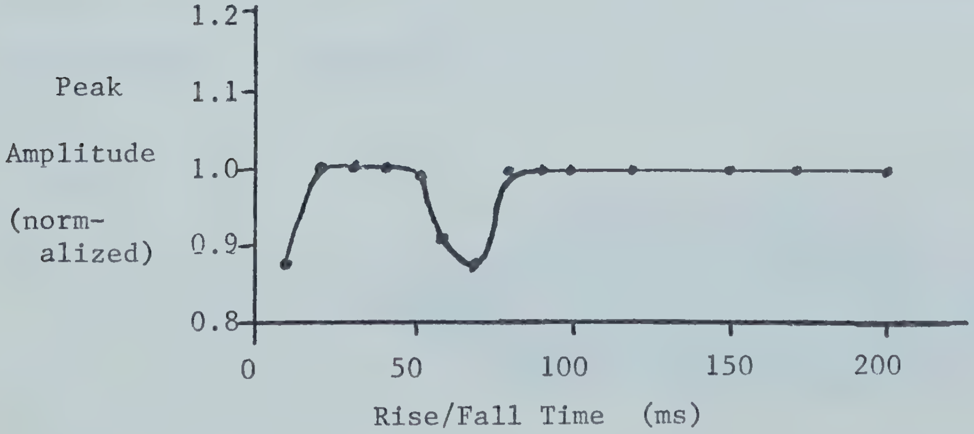


Figure 5.8 Trapezoid Peak Amplitude Performance

5.3 Tone Burst Performance

The tone burst generator would ideally not have any sinusoid output when a tone burst was not desired. However, only a limited amount of carrier suppression can be achieved. Other generators have been constructed with varying success with carrier suppression[10,11]. The more sucessful methods tend to be complex and costly. A plot of carrier suppression versus frequency is given in Figure 5.9.

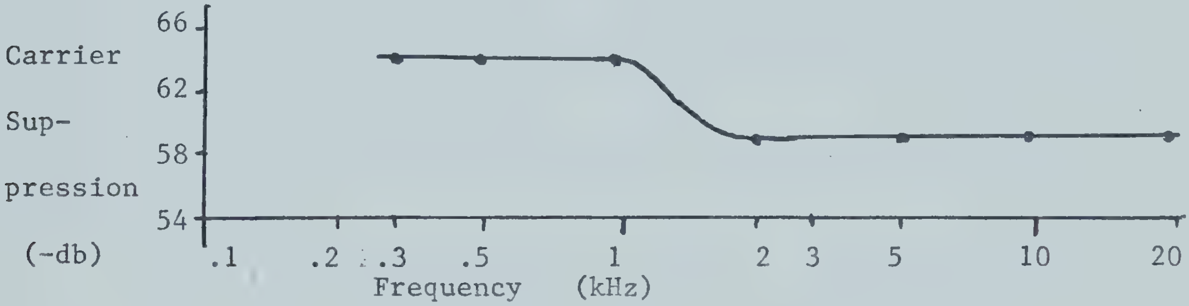


Figure 5.9 Carrier Suppression

The tone burst was to start and end at a point of zero phase relative to the sine wave carrier. A tone burst was triggered and the resulting waveform recorded with a storage oscilloscope. The waveform is reproduced in Figure 5.10.

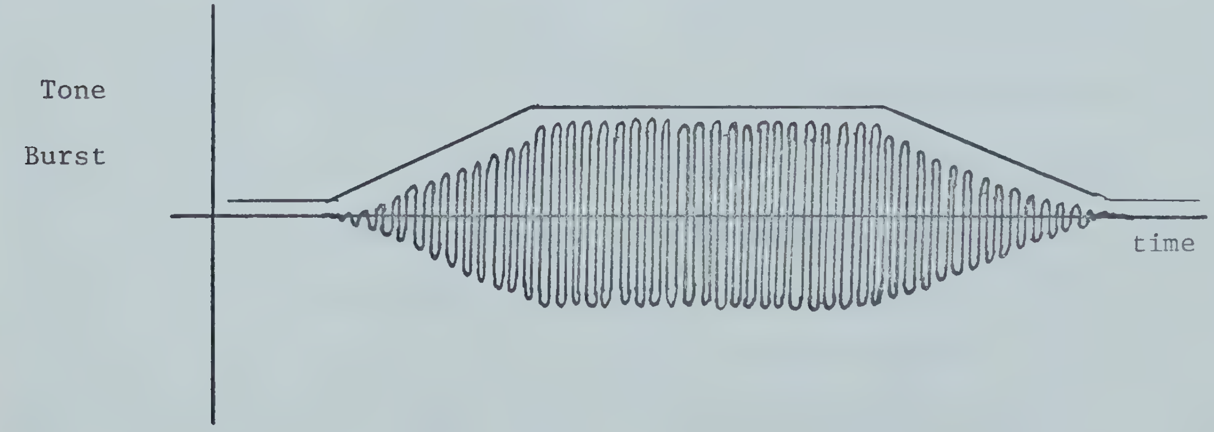


Figure 5.10 Tone Burst

CHAPTER 6

CONCLUSION

6.1 Conclusion

It was desired to construct a device which was capable of generating trapezoidally modulated tone bursts. This has indeed been accomplished. Chapter 2 of this work shows how the device was organized in order to satisfy the requirements placed upon it. Chapter 3 shows the analysis of the phase locked loop which was used in the device. Chapter 4 gives detailed circuit descriptions of some of the more novel circuits used in the construction of the device. Further circuit details of other circuits used in the device are given in Appendix C.

The device was evaluated in Chapter 5. Various graphs that illustrate the tone burst generator's performance are shown in Chapter 5. The linearizing assumptions made, regarding the voltage controlled oscillator and the phase comparator, were shown to be very reasonable. The rapid roll-off of the frequency response is unavoidable. This rapid roll-off does not seriously affect the generator's usefulness, as the acoustic transducers that are to be used with this device are highly nonlinear and a calibration curve must be used with these devices. The phase locked loop settling times are longer than the analysis in Chapter 3 would suggest. This fact limits the rapidity at which a tone burst can be triggered after a change in carrier frequency. The long settling times are particularly limiting at higher values of carrier frequency. The

trapezoid generator proved to have very reasonable performance. The carrier suppression was comparable to that of other devices which have been constructed.

6.2 Suggestions for Further Work

Several improvements can be made in the system. An obvious extension is the inclusion of other waveforms, in addition to the trapezoid, to modulate the sine wave. It would be a relatively simple task to include additional circuits to generate such waveforms as a guassian waveform, etc. The desired envelope signal could be selected by switching.

A GO/NO GO circuit would also be useful. This circuit would determine if an integral number of cycles of the sinusoid would exactly "fit" within the trapezoid. This circuit would be required to perform a division using digital circuitry. This is not a simple task and considerable additional circuitry would be required.

The rise/fall times and duration time are selected manually. Additional circuitry could be added to enable these parameters to be externally controlled.

APPENDIX A

CALCULATION OF THE BURST FOURIER TRANSFORM

For a given sine wave, $\sin(\omega_0 t + \phi)$, where ω_0 is the angular frequency, t is time, and ϕ is the phase angle, and an arbitrary envelope signal, x(t), the composite signal (or tone burst), b(t), will be given by:

$$b(t) = \left[x(t)\right]\cdot\left[\sin(\omega_0 t + \phi)\right]$$

Then,

$$\mathfrak{F}\left\{b(t)\right\} = \mathfrak{F}\left\{x(t) \cdot \sin(\omega_0 t + \phi)\right\} \qquad \text{(Equ. A.1)}$$

where $\mathfrak{F}\{\}$ represents the Fourier transform.

Let $\mathfrak{F}\left\{b(t)\right\} = B(\omega)$

and $\mathfrak{F}\left\{x(t)\right\} = X(\omega)$

where ω is the frequency variable

Equation A.1 can be written as:

$$B(\omega) = \mathfrak{F}\left\{x(t)\right\} * \mathfrak{F}\left\{\sin(\omega_0 t + \phi)\right\} \qquad \text{(Equ. A.2)}$$

where * represents convolution

Equation A.2 can be expanded to give:

$$B(\omega) = \left[X(\omega)\right] * \mathfrak{F}\left\{(\sin\omega_0 t)(\cos\phi) + (\cos\omega_0 t)(\sin\phi)\right\}$$

For any given burst, ϕ will be a constant. Thus, the trigonometric functions of ϕ will also be constants and can be removed from under the Fourier transform operator. This yields:

$$B(\omega) = \left[X(\omega)\right] * \left[(\cos\phi)\,\mathfrak{F}\left\{\sin\omega_0 t\right\} + (\sin\phi)\,\mathfrak{F}\left\{\cos\omega_0 t\right\}\right]$$

Completing the transform operations gives:

$$B(\omega) = \left[X(\omega)\right] * \left\{(\cos\phi)(\pi/j)\left[\delta(\omega - \omega_0) - \delta(\omega + \omega_0)\right] + (\sin\phi)(\pi)\left[\delta(\omega - \omega_0) + \delta(\omega + \omega_0)\right]\right\}$$

where $\delta(\omega)$ is the Dirac delta function.[4]

Performing the convolution gives:[5]

$$B(\omega) = (\cos\phi)(\pi/j)\left[X(\omega-\omega_o) - X(\omega+\omega_o)\right] + (\sin\phi)(\pi)\left[X(\omega-\omega_o) + X(\omega+\omega_o)\right]$$

APPENDIX B

CALCULATION OF LOOP FILTER RESPONSE

The phase locked loop employs a filter designated F(s). This filter was constructed as an active filter, that is, an operational amplifier was used to implement the required transfer function. The circuit is illustrated in Figure B.1.

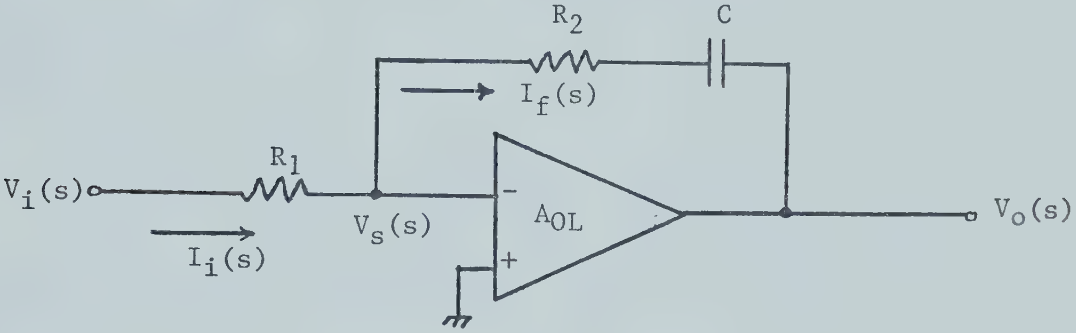


Figure B.1 Illustration of the Filter Circuit

where,

$V_i(s)$ = the Laplace transform of the input voltage

$V_o(s)$ = the Laplace transform of the output voltage

$V_s(s)$ = the Laplace transform of the summing juncton voltage

$I_i(s)$ = the Laplace transform of the input current

$I_f(s)$ = the Laplace transform of the feedback current

A_{OL} = the open loop gain of the operational amplifier

s = the Laplacian variable

R_1 = the resistance of the input resistor

R_2 = the resistance of the feedback resistor

C = the capacitance of the capacitor

Assuming that the input impedance of the operational amplifier is very large, then the input current will equal the feedback current. This gives:

$$I_i(s) = I_f(s)$$

or

$$\left[\frac{V_i(s) - V_s(s)}{R_1}\right] = \left[\frac{V_s(s) - V_o(s)}{R_2 + 1/sC}\right]$$

But $V_s(s) = V_o(s)/A_{OL}$

Therefore:

$$\frac{V_i(s)}{R_1} + \frac{V_o(s)}{A_{OL}R_1} = \frac{-V_o(s)/A_{OL}}{R_2 + 1/sC} - \frac{V_o(s)}{R_2 + 1/sC}$$

This expression can be approximated if A_{OL} is very large. This result is:

$$\frac{V_o(s)}{V_i(s)} = \frac{(sCR_2 + 1)}{sCR_1} = \frac{R_2}{R_1}\left[\frac{s + 1/R_2C}{s}\right] = F(s)$$

But $F(s) = k_f(s + a)/s$

Therefore:

$$a = 1/R_2C$$

and $$k_f = R_2/R_1$$

APPENDIX C

ADDITIONAL CIRCUIT DETAILS

C.1 Introduction

The circuit details of the more novel circuits used in the tone burst generator were given in Chapter 4. This appendix gives the circuit details of the circuits that are of a more standard nature.

C.2 The Local Oscillator

This oscillator was crystal controlled to ensure frequency stability. A schematic diagram of this circuit is shown in Figure C.1.[8]

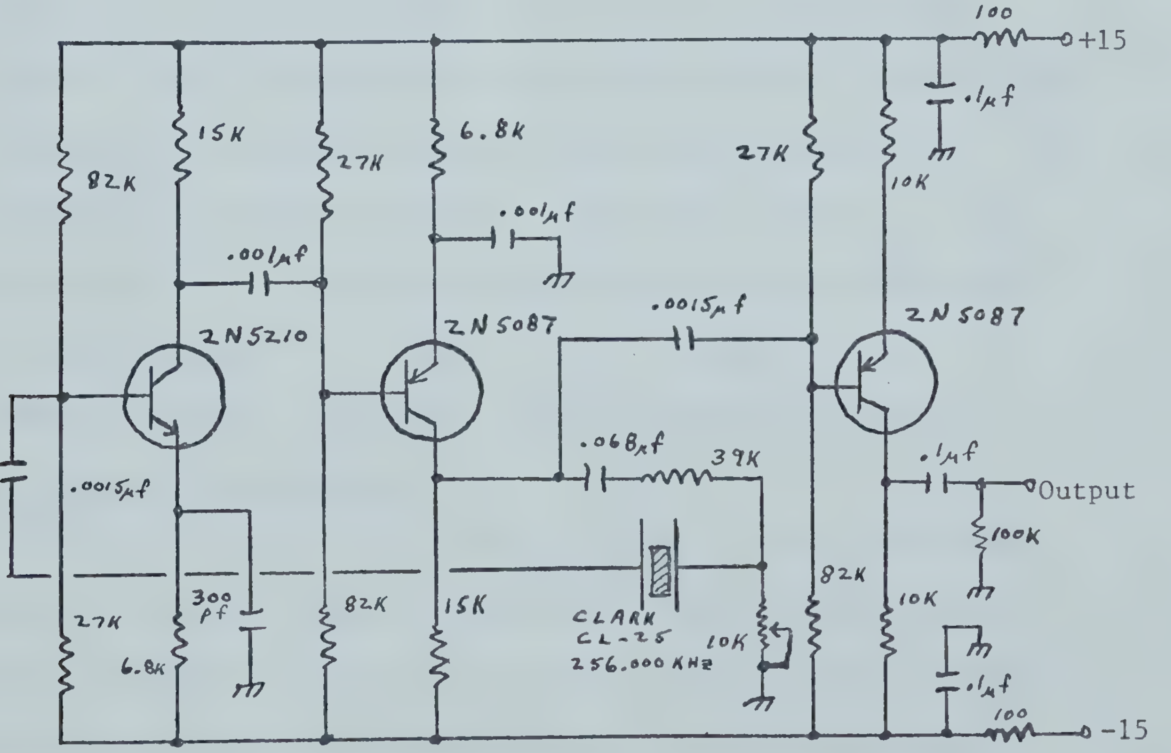


Figure C.1 Schematic Diagram of the Local Oscillator

C.3 The Mixer

A mixing operation is an analog multiplication process. Consequently, an integrated circuit multiplier was used to perform this operation. The basic system is illustrated in Figure C.2.

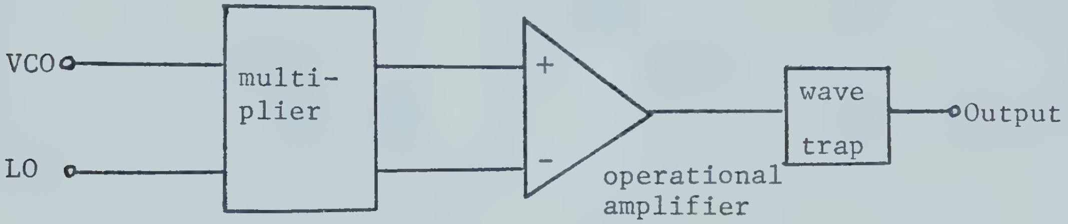


Figure C.2 Basic Mixer Layout

The multiplier accepts inputs from the voltage controlled oscillator and from the local oscillator. These signals are multiplied together. This operation produces both sum and difference frequencies. Low pass elements are included in the multiplier circuitry and in the operational amplifier circuit to suppress the sum frequency. The multiplier provides a differential output. The operational amplifier was used to convert this signal to a single ended signal. The wave trap was included to suppress any signals that feed through to the output from the multiplier inputs. A schematic diagram of the mixer circuit is given in Figure C.3.

C.4 The Schmitt Triggers

The outputs of the local oscillator and the mixer are required to drive digital circuitry but are sinusoidal in nature. Thus, two Schmitt triggers were required. The square wave outputs must have very fast fall times to operate the digital circuitry. Consequently, integrated circuit logic gates were used to square

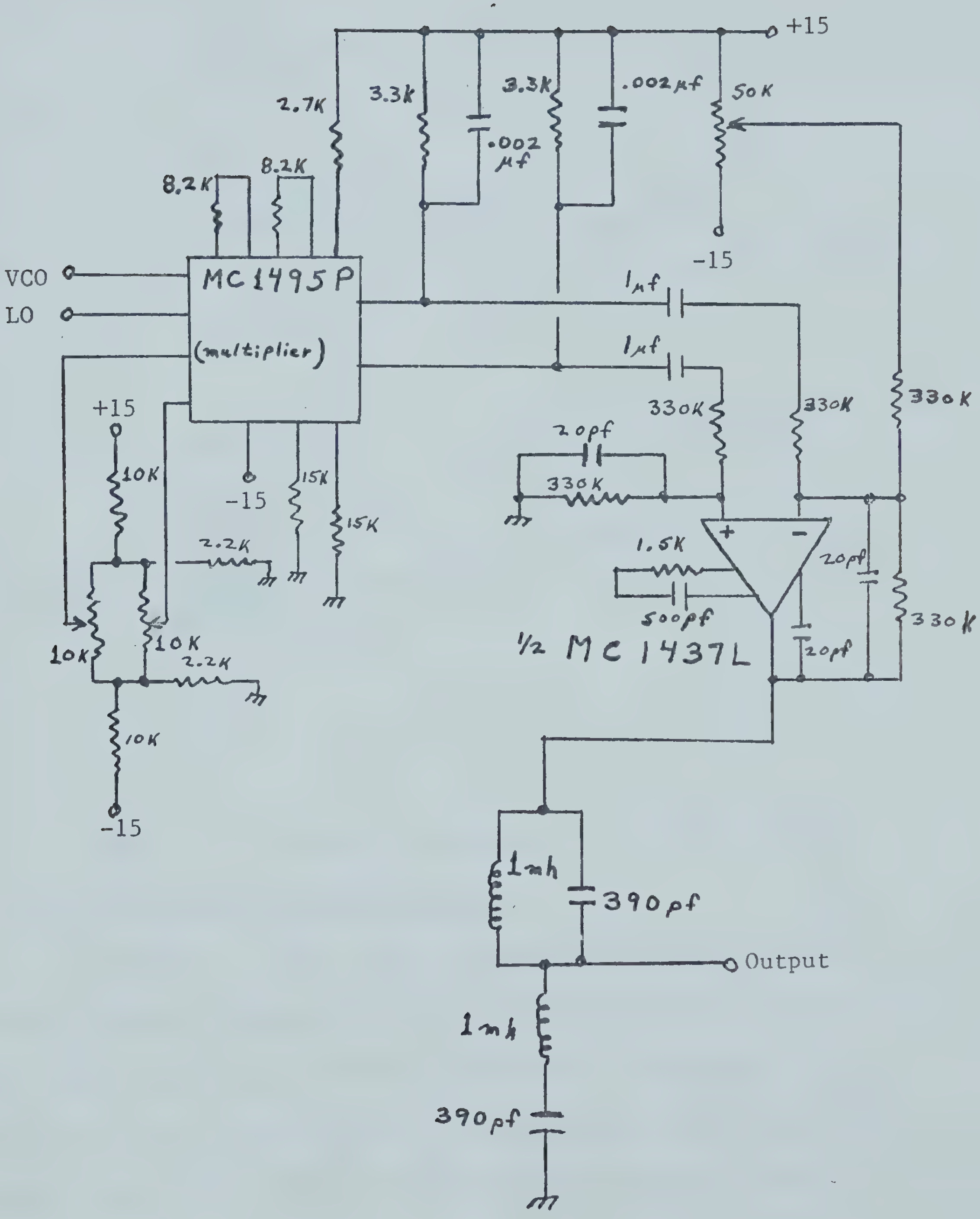


Figure C.3 Schematic Diagram of the Mixer

the input sine waves. Schematic diagrams of the Schmitt triggers are given in Figure C.4.

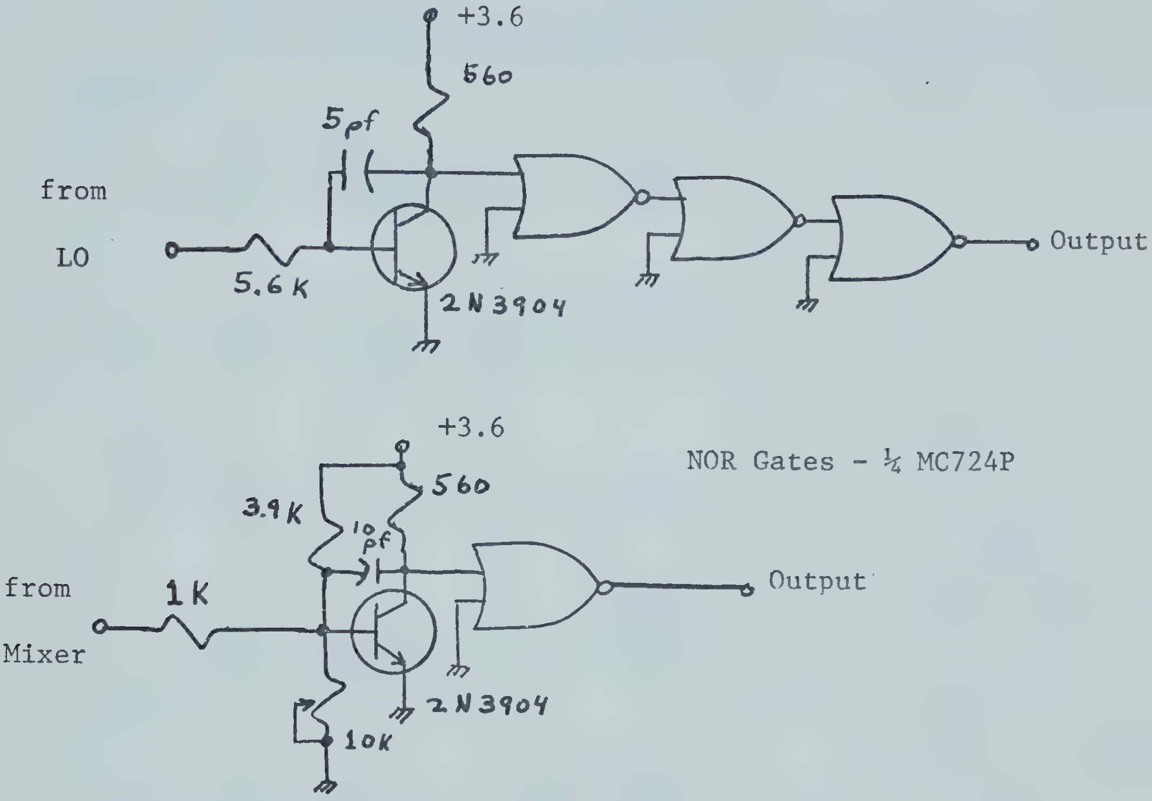


Figure C.4 Schematic Diagrams of the Schmitt Triggers

C.5 The ÷N Digital to Analog Converter

The output of this digital to analog converter is used to coarse tune the voltage controlled oscillator. The converter uses a weighted summing network to achieve the conversion. The digital inputs are obtained from the programming of the ÷N counter. Since the programming inputs can arise from an external source, logic gates are used to buffer the inputs. A schematic diagram of the converter is shown in Figure C.5.

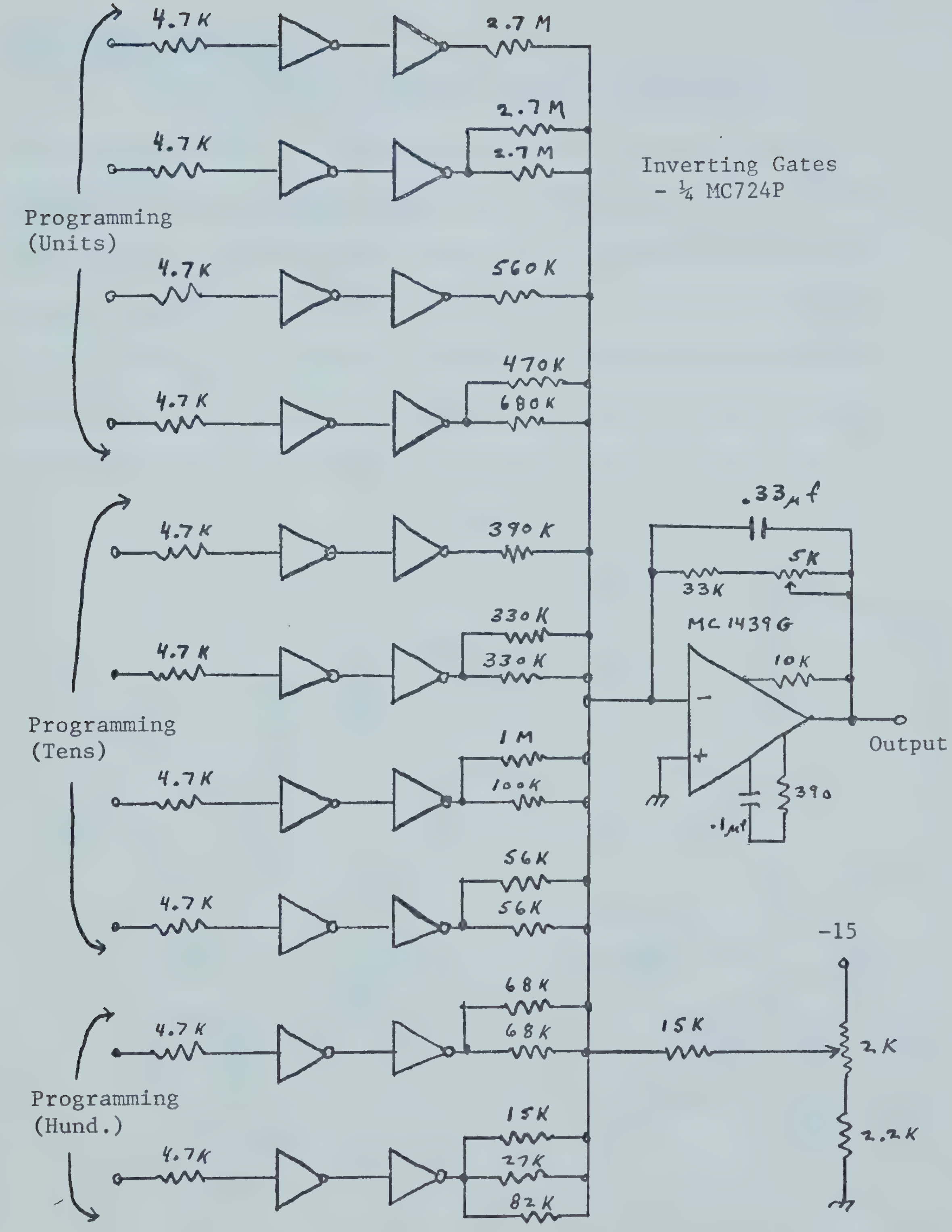


Figure C.5 Schematic Diagram of the ÷N Digital to Analog Converter

C.6 The Modulator

This circuit is required to amplitude modulate the sinusoid generated by the phase locked loop with the trapezoid generated by the trapezoid generator. Since amplitude modulation is an analog multiplication process, an integrated circuit multiplier was used to perform this operation. A schematic diagram of the modulator is shown in Figure C.6. The multiplier performs the modulation while the operational amplifier is used to convert the multiplier's differential output to a single ended output.[9]

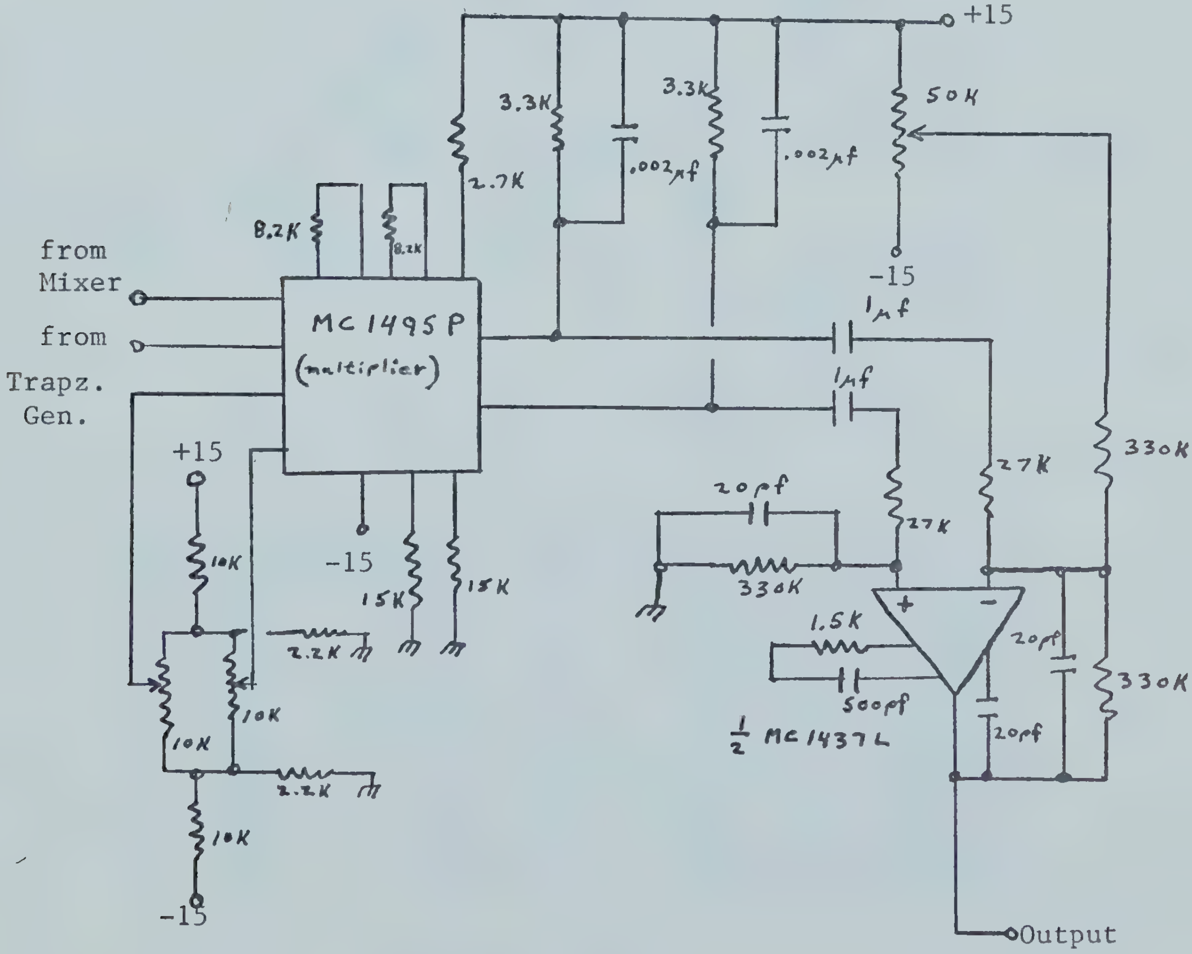


Figure C.6 Schematic Diagram of the Modulator

C.7 The Power Amplifiers

Two power amplifiers were required. The amplifiers are of an operational amplifier configuration. A schematic diagram of one of the power amplifiers (they are identical) is shown in Figure C.7. Table C.1 shows the output power as a function of the feedback element.

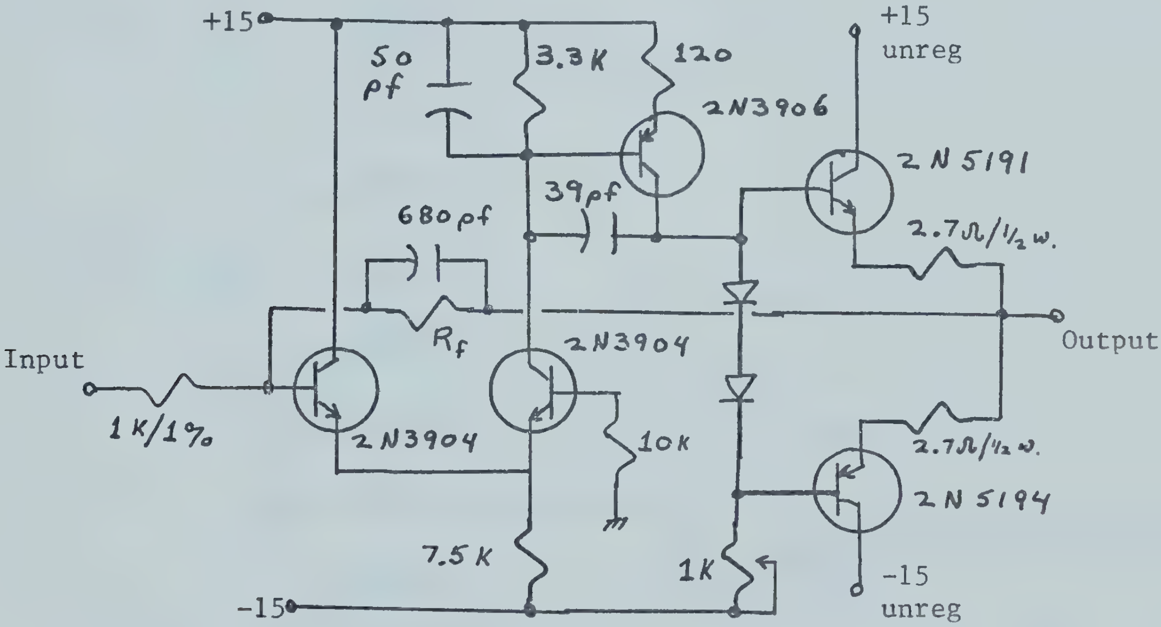


Figure C.7 Schematis Diagram of the Power Amplifiers

Switch Setting	Power Level	Power Level	R_f
00	0 db	50 µw	221 Ω
10	5 db	158 µw	392 Ω
20	10 db	500 µw	698 Ω
30	15 db	1.58 mw	1.21 k
40	20 db	5.0 mw	2.21 k
50	25 db	15.8 mw	4.02 k
60	30 db	50 mw	7.5 k
70	35 db	158 mw	14.0 k
80	40 db	500 mw	27.4 k
90	45 db	1.58 w	69.8 k

Table C.1 Output Power Levels

C.8 The Rise/Fall Digital to Analog Converter

This digital to analog converter uses a weighted summing network to achieve the conversion. The digital inputs are obtained from the programming of the Rise/Fall counter. A schematic diagram of this circuit is shown in Figure C.8.

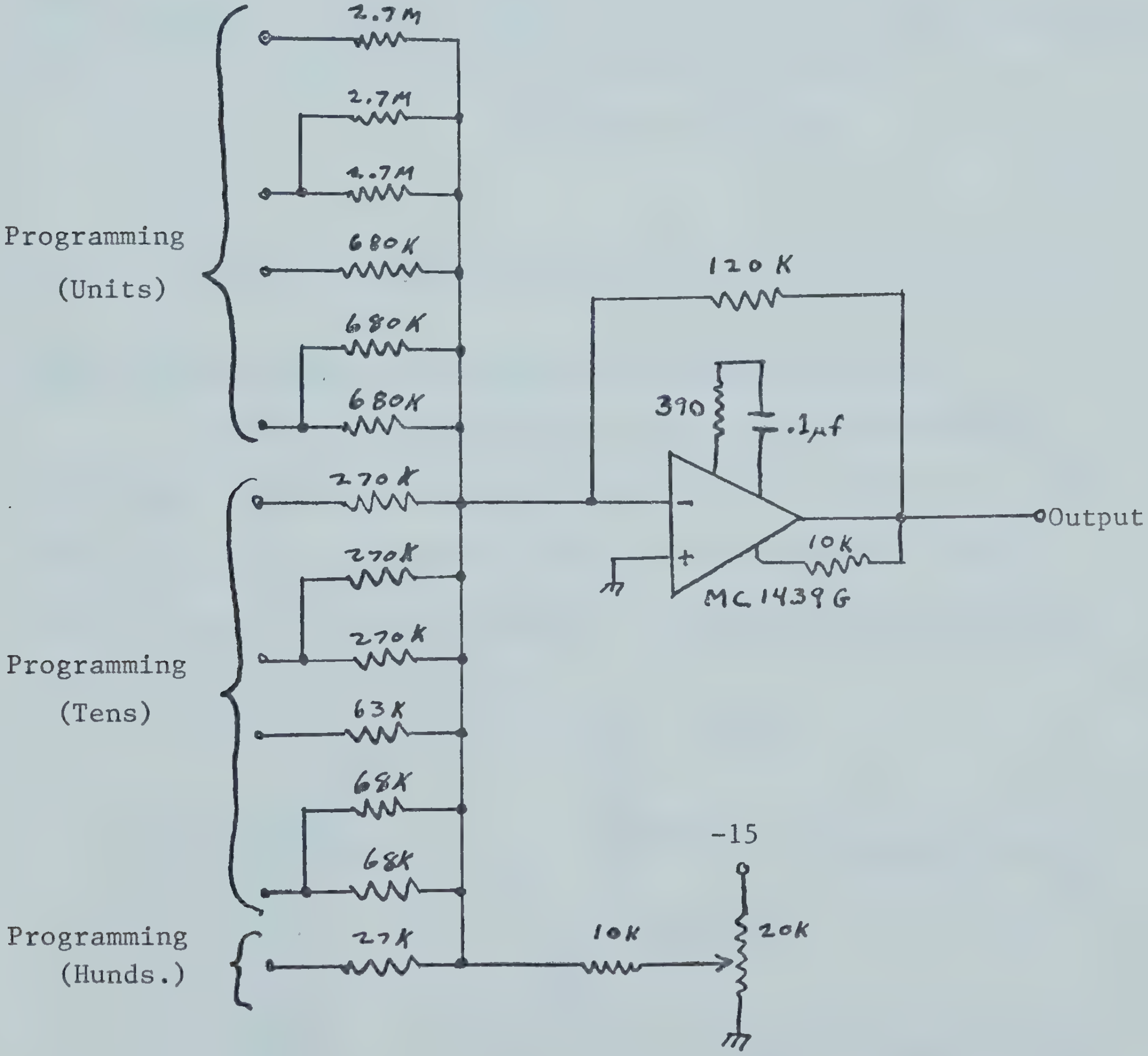


Figure C.8 Schematic Diagram of the Rise/Fall Digital to Analog Converter

C.9 The Reference Frequency Prescaler

This circuit divides the local oscillator frequency down to give the reference frequency input to the phase comparator. A schematic diagram of this circuit is shown in Figure C.9.

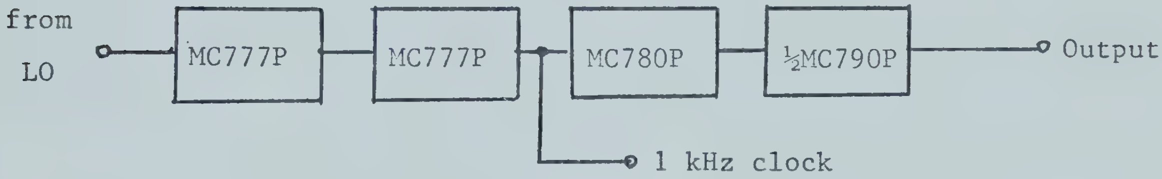


Figure C.9 Schematic Diagram of the Reference Prescaler

C.10 The Unijunction Oscillator and Antibounce Circuit

In the AUTO trigger mode, trigger pulses are obtained from a local low frequency unijunction transistor oscillator. This oscillator can be set to have a pulse repitition rate of from 1 pulse/second to 1 pulse/9 seconds. A schematic diagram of this circuit is given in Figure C.10.

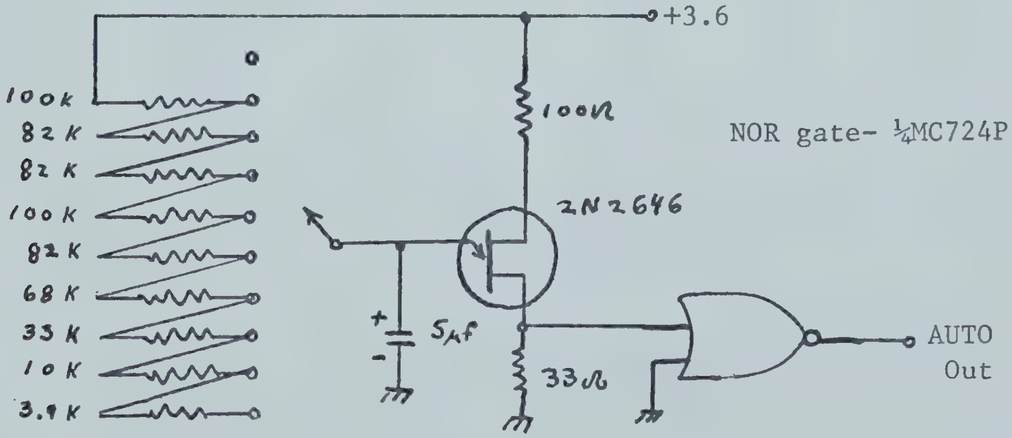


Figure C.10 Schematic Diagram of the Unijunction Transistor Oscillator

In the MANUAL trigger mode, trigger pulses are obtained from a manual pushbutton. An antibounce circuit is required to prevent sporadic triggering that would result from the pushbutton contact bounce. This circuit is illustrated in Figure C.11.

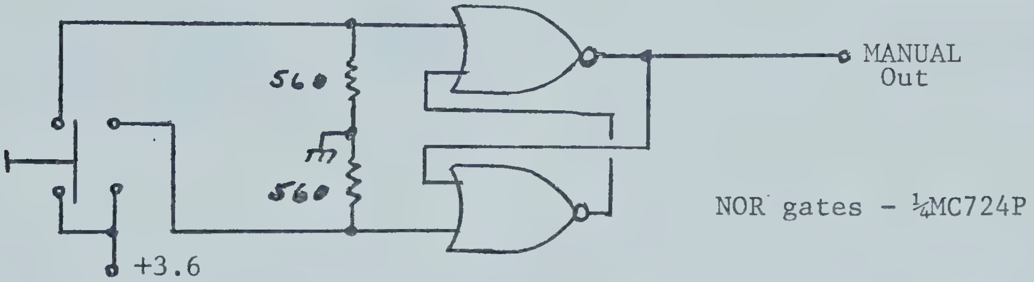


Figure C.11 Schematic Diagram of the Antibounce Circuit

C.11 The +3.6 vdc Power Supply

A +3.6 vdc power supply is required to operate the digital circuitry used in the tone burst generator. A schematic diagram of this circuit is shown in Figure C.12.

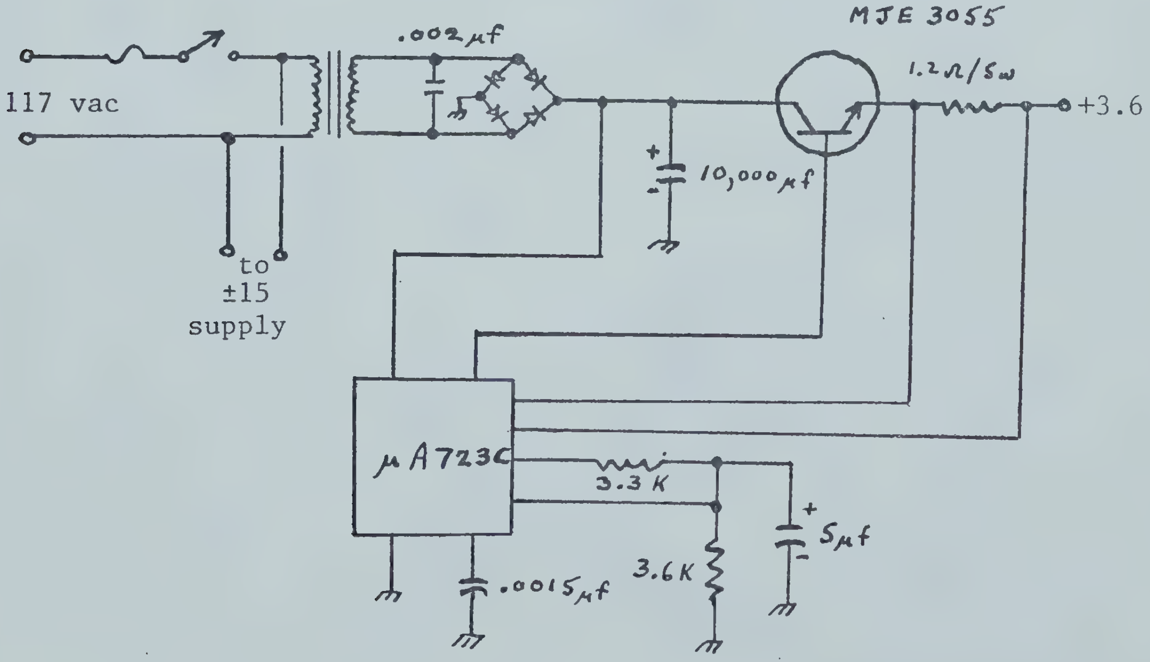


Figure C.12 Schematic Diagram of the +3.6 vdc Power Supply

C.12 The ±15 vdc Power Supply

The analog circuitry used in the tone burst generator operates from ±15 vdc power supply. A schematic diagram of this circuit is given in Figure C.13.

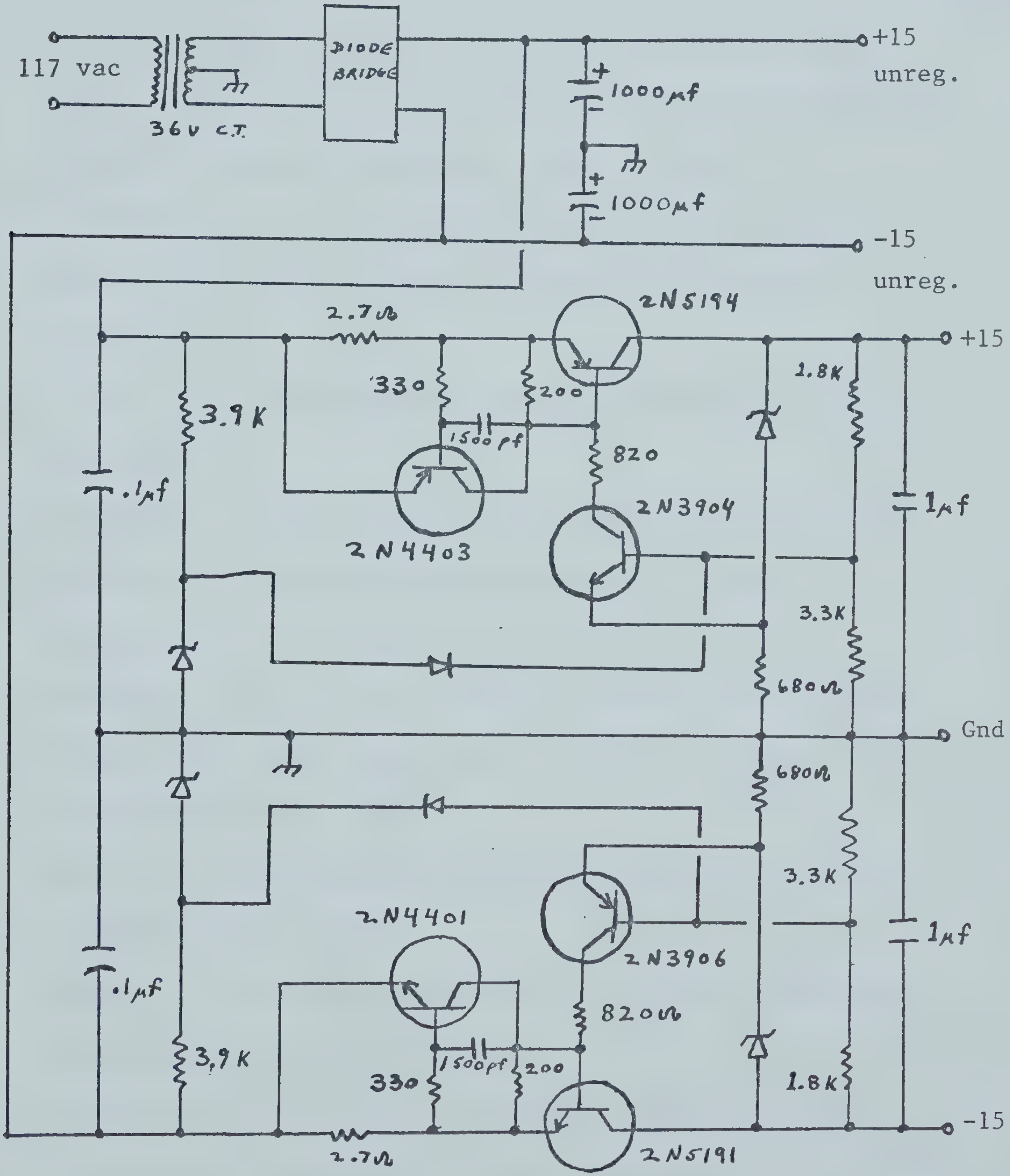


Figure C.13 Schematic Diagram of the ±15 vdc Power Supply

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